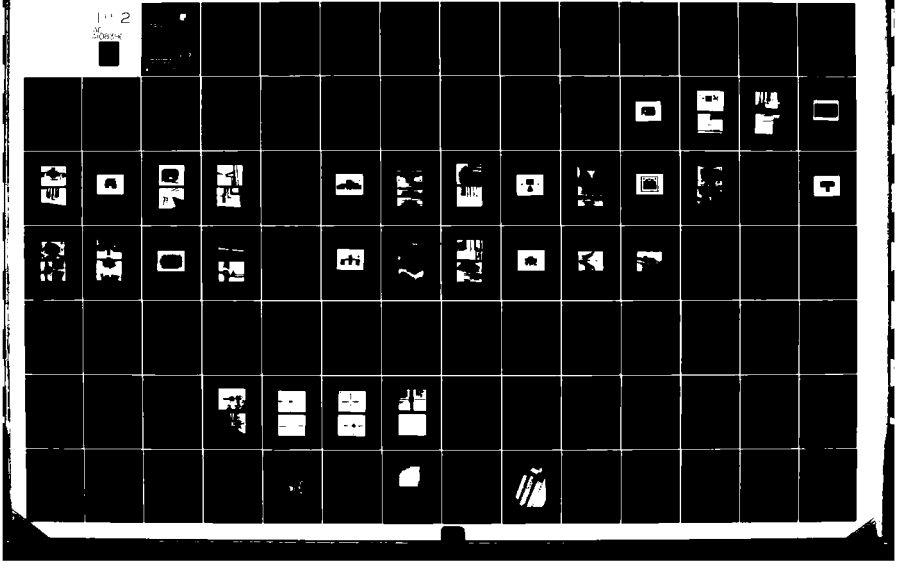
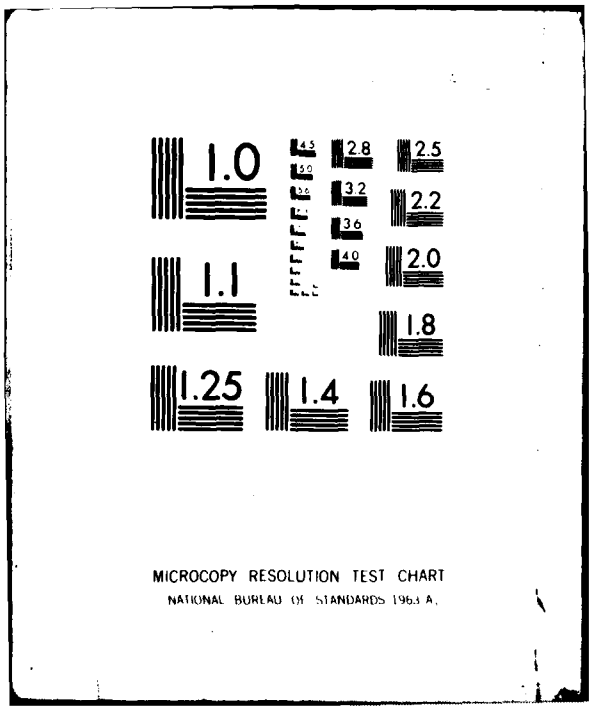
AD-A108 396 HUGHES AIRCRAFT CO TORRANCE CA TORRANCE RESEARCH CENTER F/G 9/1
RELIABILITY INVESTIGATION OF LOW NOISE GAAS FETS.(U)
JUL 81 L S BOWMAN, W TARN F30602-78-C-0295
UNCLASSIFIED HAC-W-43413 RADC-TR-81-181 NL




1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A.

RADC-TR-81-181
Final Technical Report
July 1981

LEVEL II

12

RELIABILITY INVESTIGATION OF LOW NOISE GaAs FETs

Hughes Aircraft Company

L. S. Bowman
W. Tam

AD A108396

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

This report has been reviewed by the [illegible] Office (PI) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be available to the general public, including foreign nations.

RADC-TR-82-182 has been reviewed and is approved for publication.

APPROVED: Edward J. Calnick
EDWARD J. CALNICK
Project Engineer

APPROVED: David C. Luke
DAVID C. LUKE, Colonel, USAF
Chief, Reliability and Compatibility Division

FOR THE COMMANDER: John P. Huss
JOHN P. HUSS
Acting Chief, Plans Office

If your address has changed or if you wish to be removed from the mailing list, or if the addressee is no longer employed by your organization, please notify RADC (RBRT), Griffiss AFB NY 13441. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document require that it be returned.

represented a broad cross section of currently available devices, and included both gold-based and aluminum gate metallizations with gate lengths nominally from 0.5 μm to 1.2 μm.

Physically, DC electrical, and microwave characterization tests of the FETs are presented first. Optical microphotographs were taken, and SEM photographs and EDAX measurements were obtained. DC electrical measurements were made of drain current, gate voltage, pinchoff voltage, transconductance, and gate diode reverse breakdown voltage. Microwave characterization included measurements of minimum noise figure and associated gain, maximum available gain, power output at 1 dB gain compression, and S-parameters from 2 GHz to 12 GHz.

A discussion of preliminary device failures and losses follows. Results of environmental characterization tests are then given. These included hermeticity, temperature cycling, acceleration, random vibration, and mechanical shock.

Chip devices comprising eight FET types from six manufacturers were subjected to high temperature accelerated stress testing at 200°C, 220°C, 240°C, and 260°C. A total of 59 FETs were temperature stressed at approximate low noise bias conditions, and 28 FETs were held at temperature unbiased. RF oscillation suppression networks were built into the gate and drain bias lines.

Packaged devices comprising eight FET types from five manufacturers were tested at 85°C, and 120°C. Among the 53 FETs in these temperature tests 29 were low noise biased and 24 were unbiased. Networks in the gate and drain bias lines suppressed any tendency toward RF oscillations. Hughes Aircraft Company is continuing these tests.

Packaged devices in an amplifier housing, along with input and output matching networks, were tested at 200°C channel temperature under DC bias with CW RF input. Unbiased FETs were also placed in the ovens as controls. These tests were begun late in the program and have not yet yielded much data. Hughes Aircraft Company is continuing this work.

Failure data on devices in the high temperature accelerated stress tests were used to make log-normal plots from which the median time to failure at the stress temperature was inferred. An Arrhenius plot on one device type is presented and the activation energy is computed. A least squares approach is used to infer the best fit to the experimental data.

Prediction is made of the median life expectancy at typical operating temperatures. Failure modes and mechanisms for both catastrophic and degradation failures are discussed, and the reliability of low noise GaAs FET devices is assessed. Failed devices from this program were delivered to the complementary Rome Air Development Center/Hughes program, "Failure Mechanism Study of GaAs FET Technology", Contract No. F30603-78-C-0326, for further work.

ACKNOWLEDGMENT

From the inception of the proposal writing through the first nineteen months of work on this contract, Glenn O. Ladd was Program Manager. Lawrence S. Bowman became Program Manager in May 1980 when Dr. Ladd transferred to another division of Hughes Aircraft Company. The authors gratefully acknowledge Dr. Ladd's many contributions to the successful completion of this program.

We acknowledge the many contributions of B. Bernor, D. Higgins, W. Klatskin, and G. Williams, who worked on the program, and the continual support of Dr. T. A. Midford, Manager of the Hughes Torrance Research Center. We have greatly appreciated the interest and encouragement of E. J. Calucci and J. Carroll of the Rome Air Development Center in accomplishing the program goals.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

LIST OF TABLES

EVALUATION

An attempt was made within this contractual effort to assess the reliability and operating life characteristics of small signal, gallium arsenide (GaAs) metal epitaxial semiconductor field-effect transistors (MESFETs). The approach was to have the contractor purchase as many devices as the contract monies would allow of prominent, off-the-shelf devices which represented a variety of vendor geometries, processing and metallizations. Appropriate tests were performed on the devices with the data and analyses providing useful reliability data for military system developers. Further, the resulting failed devices were to be analyzed in greater detail under another contractual program with the same contractor entitled, "Failure Mechanism Study of GaAs FET Technology." Further accelerated stress test data will be necessary to assess and establish the reliability and operating life of small signal GaAs FETs. Since this study did not fully meet its original goals, the reader is cautioned that the data resulting from this program may have limitations.

EDWARD J. CALUCCI
Reliability Physics Section
Reliability Branch

1.0 INTRODUCTION

This is the final report covering Hughes Aircraft Company's work during the period from 31 August 1978 through 31 August 1980 on Rome Air Development Center Contract No. F30602-78-C-0295. The objective of this program is to assess the reliability and operating life characteristics of low noise, small signal, microwave, n-channel, gallium arsenide (GaAs), metal-epitaxial-semiconductor field effect transistors (MESFETs) with a Schottky-barrier gate, and to identify associated failure mechanisms. Commercially available devices from prominent domestic and foreign sources representative of current military needs have provided the basis for this investigation. Diverse types of low noise FETs were selected to allow us to examine a cross section of device types and processing methods.

Failed devices from this program were delivered to the companion Rome Air Development Center/Hughes program, "Failure Mechanism Study of GaAs FET Technology," Contract No. F30602-78-C-0326, for additional failure analysis work.[1]

2.0 PROCUREMENT AND CHARACTERIZATION OF LOW NOISE FET DEVICES

The devices procured for this program are representative of commercial devices available at the time of procurement (second half of 1978). A sample of most chip types was optically photographed and examined in the Scanning Electron Microscope (SEM). X-ray analysis (EDAX) was used where needed to establish constituents of the metallization. Representative pictures and commentary of the FET types are given. DC and microwave characterization information follows.

2.1 FET SELECTION

A total of 326 chip devices and 151 packaged FETs was procured for the program. There are 23 device types from 7 manufacturers. Table 2-1 shows the list of devices and the tests to which they were submitted. Actual manufacturer's part numbers are not shown, at the request of the Contracting Officer. Instead, an arbitrary code designation has been specified for every individual type of device in Table 2-1. "Type Code" refers to the assigned designation of each FET type. The Type A-10 devices were made by a different manufacturer from the other A-type FETs. The other unique initial letters in the type code assignment correspond to specific manufacturers.

In Table 2-1 "Initial Inv" refers to the initial inventory of FETs obtained for the program. "Prelim Losses" refers to devices that were lost or found unsuitable for the tests. These are discussed in Section 3. One chip of each device type was subjected to "SEM/EDAX" examination. "Envir Tests" refers to environmental characterization tests that are discussed in Section 4. "High T Stress" refers to the constant temperature tests on chips done at 200°C, 220°C, 240°C, or 260°C that are discussed in Section 5. "Med T Stress" refers to the constant temperature tests on packaged FETs done at 85°C and 120°C that are discussed in Section 6. "RF Stress" refers to the RF stress tests that are discussed in Section 7. FETs that are held in reserve are listed in the "Not Commit" column.

At the beginning of the program several other advertised FET types were sought for purchase from their vendors. Three of these were withdrawn from the market before they could be purchased. In some cases improved versions of FET types became available during the course of the program, and we were able to acquire them for

TABLE 2-1

INITIAL INVENTORY AND DISPOSITION OF FETS

Type Code	Initial Inventory		Prelim Losses	SEM/ EDAX	Envir Tests	High T Stress	Med T Stress	RF Stress	Other Tests	Not Commit
	Chip	Pkg								
A-1	50		50							
A-6	50		15			32			3	
A-51		10	4				6			
A-10	15		6	1		8				
D-1	11		3	1		7				
D-11		9			2			5		2
D-2	11		5	1		5				
D-22		11	2		2		4		2	1
H-1	76		21	1		27			5	22
H-11	15		2			13				
H-1A1		21	2		2		9	5		3
H-21		21	3		2		10			6
Page Total	228	72	113	4	8	92	29	10	10	34
Program Total										

TABLE 2-1 (Cont)

INITIAL INVENTORY AND DISPOSITION OF FETS

Type Code	Initial Inventory		Prelim Losses	SEM/ EDAX	Envir Tests	High T Stress	Med T Stress	RF Stress	Other Tests	Not Commit
	Chip	Pkg								
N-2	10		9	1						
N-21		21			2		6			13
N-3	61		5	1		40				15
N-31		31	8		2		9			12
N-32		11					6	3		2
P-4	3			1						2
P-5	11		5	1		5				
P-51		6	1		2					3
R-2	2		1	1						
R-5	11		10	1						
R-51		10	1		2		3	4		
Page Total	98	79	40	6	8	45	24	7		47
Program Total	326	151	153	10	16	137	53	17	10	81

testing. Specifically, 50 Type A-6 FETs were supplied by the vendor at no cost to Hughes as replacements for their Type A-1 devices, and 15 Type H-11 FETs were supplied by their vendor as an improvement over their Type H-1 FET.

Section 3 discusses the reasons behind these substitutions. Additional discussion is given in Section 5.4, including an explanation of the relatively large numbers of uncommitted chips of Type H-1 (22 units) and Type N-3 (15 units).

The only other types with appreciable numbers of uncommitted devices are the N-21 (13 units) and N-31 (12 units), both packaged FET types. These were procured for possible additional tests which, as it turned out, were not needed to complete the program goals.

Table 2-2 is a compilation of vendor's data for the grounded source configuration, where standard notations are used for the various parameters. Data are given for 18 of the 23 device types. Not represented are FET types D-2, N-21, N-32, P-51, and R-51.

2.2 PHYSICAL CHARACTERISTICS

The FET types for this program were selected to offer a variety of styles of construction, including both aluminum and gold-based gate metallizations. Table 2-3 shows important physical characteristics of the low noise FETs. Gate lengths of the devices range from 0.5 to 1.2 μm, and different gate geometries are represented. Source, drain, and chip measurements are also given. Reference to Tables 2-2 and 2-3 will aid in interpreting the results given in this report.

2.3 SEM/EDAX EXAMINATIONS

Ten low noise FET chips were given SEM/EDAX examinations at the Hughes Components and Materials Laboratories in Culver City, California. Detailed descriptions and SEM pictures follow.

TABLE 2-2

MANUFACTURER'S SPECIFICATIONS

Type Code	A-10	A-1	A-6	A-51	D-1	D-11	D-22	H-1	H-1A1	H-11
TYP. PARAMETERS										
f, GHz	8	4	12	4	8	7	7	10	4	10
F_{min}, dB/G_a, dB	2.7/9	1.3/12	2.5/9	1.3/12	2.7/8	3.3/10.5	3.0/10.5	3.6/6.9	1.6/11	3.2/6.9
at I_D, mA/V_D, V	10/3	20/3	10/3	20/3	20/3.5	15/3.5	15/3.5	12/3.5	12/3.5	12/3.5
P_o, mW/G, dB	63/-	50[1]/-	10[1]/-	50[1]/-	-/-	25/-	-	28/-	35/10.5	30/-
at I_D, mA/V_D, V	0.5 I_{DSS}/3	50/5	40/5	50/5	-/-	30/6	-	30/4	30/4	30/4
G_{max}, dB	11	12[2]	12	12[2]	-	12	12	11	16	11
at I_D, mA/V_D, V	I_{DSS}/3	I_{DSS}/3	40/3	I_{DSS}/3	-	60/3.5	60/3.5	60/4	60/4	60/4
I_{DSS}, mA/V_D, V	80/3	120/3	50/3	120/3	60/3	60/3	-/-	60/4	60/4	60/4
g_m, mmho	30	65	30	65	35	35	22	45	40	45
at I_D, mA/V_D, V	65/3	I_{DSS}/3	50/3	I_{DSS}/3	60/3	60/3	60/3	50/4	50/4	50/4
V_P, V	-3	-2	-2	-2	-3	-3	-3	-2	-2	-2
at I_D, μA/V_D, V	100/3	1000/3	1000/3	1000/3	1000/3	1000/3	1000/3	100/4	100/4	100/4
θ_j, °C/W	50	200	-	200	70	-	-	100	200	100
MAX RATINGS										
V_D, V	5	7	5	7	8	10	10	5	5	11
V_G, V	-5	-5	-4	-5	-8	-8	-8	-5	-5	-10
P_{DISS}, mW	500	500	200	500	800	500	500	-	-	-
T_{ch}, °C	125	125	150	125	175	140	140	125	125	300

NOTES: 1. P_o at 1 dB gain compression. 2. f = 6 GHz.

TABLE 2-2 (CONTINUED)

MANUFACTURING SPECIFICATIONS

Type Code	H-21	N-2	N-3	N-31	P-4	P-5	R-2	R-5
TYP. PARAMETERS								
f, GHz	10	8	8	8	8	10	10	10
F_{min}, dB/G_a, dB	2.4/9.2	3.0/-	2.0/11.5	2.3/11.0	3.0/8	3.0/7	-/-	3.0/7
at I_D, mA/V_D, V	7.5/3.5	10/3	10/3	10/3	10/5	10/5	-/-	10/4
P_o, mW/G, dB	16/12	7[1]/10	7/12	7/12	-/-	-/-	200/6.5	8[1]/-
at I_D, mA/V_D, V	0.5 I_{DSS}/3.5	30/3	30/3.0	30/3.0	-/-	-/-	0.5 I_{DSS}/12	0.5 I_{DSS}/4
G_{max}, dB	14.5	11	14	13	10	10	8	10
at I_D, mA/V_D, V	I_{DSS}/3.5	30/3	30/3	30/3	-/-	-/-	80/12	I_{DSS}/4
I_{DSS}, mA/V_D, V	50/3.5	60/3	55/3	55/3	≤100/5	≤100/5	140/4	40/4
g_m, mmho	32	20	25	25	-	-	40	35
at I_D, mA/V_D, V	I_{DSS}/3.5	30/3	30/3	30/3	-/-	-/-	80/4	I_{DSS}/4
V_P, V	-2	-4	-2.5	-2.5	-5	-5	-4.5	-2
at I_D, μA/V_D, V	500/3.5	100/3	100/3	100/3	10/5	10/5	1000/4	100/4
θ_j, °C/W	230	-	170	250	-	-	-	-
MAX RATINGS								
V_D, V	4	5	5	5	6	6	15	6
V_G, V	-4	-10	-10	-10	-10	-10	-5	-5
P_{DISS}, mW	-	500	500	500	500	500	2000	500
T_{ch}, °C	125	125	175	175	-	-	125	125

NOTES: 1. P_o at 1 dB gain compression. 2. f = 6 GHz.

TABLE 2-3

IMPORTANT PHYSICAL CHARACTERISTICS OF LOW NOISE FET DEVICES

Type Code	Initial Inv		Gate Metal	Gate Length, μm	Gate Pads	Gate Geometry	Gate Finger Width μm	Gate Width μm	Source-Drain Spacing μm	Source Width μm	Drain Width μm	Chip Size μm
	Chip	Pkg										
A-10	15		Alum.	1.0	1	Two parallel fingers	120	240	4	50	17	305 x 200
A-1	50		Gold	0.5	4	28 Parallel fingers	25	700	2	8	8	480 x 380
A-51		10	Gold	0.5	4	28 Parallel fingers	25	700	2	8	8	480 x 380
A-6	50		Gold	0.5	1	Linear	400	400	2	37	8	550 x 380
D-1	11		Gold	1.0	2	Linear	400	400	5	130	15	500 x 300
D-11		9	Gold	1.0	2	Linear	400	400	5	130	15	500 x 300
D-2	11		Gold	0.75	1	Linear	200	200	4	100	15	305 x 285
D-22		11	Gold	0.75	1	Linear	200	200	4	100	15	305 x 285
H-1	76		Alum.	1.0	1	Linear	400	400	5	85	16	565 x 250
H-11	15		Alum.	1.0	1	Linear	500	500	5	100	20	630 x 310
H-1A1		21	Alum.	1.0	1	Linear	400	400	5	85	16	560 x 250
H-21		21	Alum.	0.5	2	Linear	200	200	5	150	16	410 x 275
N-2	10		Alum.	1.0	1	V-shape	140	280	3	Tapered	Tapered	400 x 400
N-21		21	Alum.	1.0	1	V-shape	140	280	3	Tapered	Tapered	400 x 400
N-3	61		Alum.	0.5	2	Linear	230	230	2	[illegible]	34	360 x 315
N-31		31	Alum.	0.5	2	Linear	230	230	2	120	34	360 x 315
N-32		11	Alum.	0.5	2	Linear	230	230	2	120	[illegible]	360 x 315
P-4	2		Alum.	1.2	1	Two parallel fingers	130	260	4	120	[illegible]	475 x 320
P-5	11		Alum.	1.0	1	Two parallel fingers	130	260	5	150	100	600 x 350
P-51		6	Alum.	1.0	1	Two parallel fingers	130	260	5	150	100	600 x 350
R-2	3		Alum.	1.0	1	Linear	200	200	8	40	16	840 x 440
R-5	11		Gold	1.0	1	Linear	230	230	5	38	38	300 x 235
R-51		10	Gold	1.0	1	Linear	230	230	5	38	38	300 x 235
Total	326	151										

Type A-10 (Figures 2-1, 2-2, and 2-3)

SEM photographs show that the gate has been etched down in several steps. The gate is aluminum, as determined from the EDAX photographs. The gate shows narrowing at its termination, where it crosses the main mesa. The aluminum metallization is badly grained, indicating a non-optimum evaporation. The gate pad is composed of titanium/platinum/gold directly overlaying the aluminum, with a thick gold pad overlaying the titanium/platinum/gold.

The source metallization EDAX scans show a thick gold bond pad under which is apparently just a titanium/gold layer overlaying what is probably a gold-germanium/nickel alloyed contact. The germanium does not appear on the EDAX scan.

There may have been some attack of the aluminum metallization after removal of the glass overlay, but it is not apparent on these photographs. The gate etching appears to have undercut slightly the source contact.

Type D-1 (Figures 2-4 and 2-5)

The EDAX scan shows that the overlay glass is partially composed of silicon. The gate metallization is relatively clean and was obviously accomplished by the lift process. The gate connector crosses a shallow sloping mesa step. SEM photographs after removal of the glass show that the gate region was etched prior to metal deposition. Also, the gate metallization is slightly undercut, perhaps by a slight etch of the underlying refractory layer after lifting. The thickness of the gate metallization appears to be somewhat less than half the gate length.

Type D-2 (Figures 2-6, 2-7 and 2-8)

This device had a large flake out of the overlay glass in the gate pad area. There are anomalies of the gallium arsenide etching in the vicinity of the gate termination. The gate appears to have been lifted, and the channel has been etched. This device also, as in the other devices from this vendor, shows some slight undercutting of the gate metallization. After removal of the overlay glass, the gate has separated from the GaAs and also has delaminated from the glass.

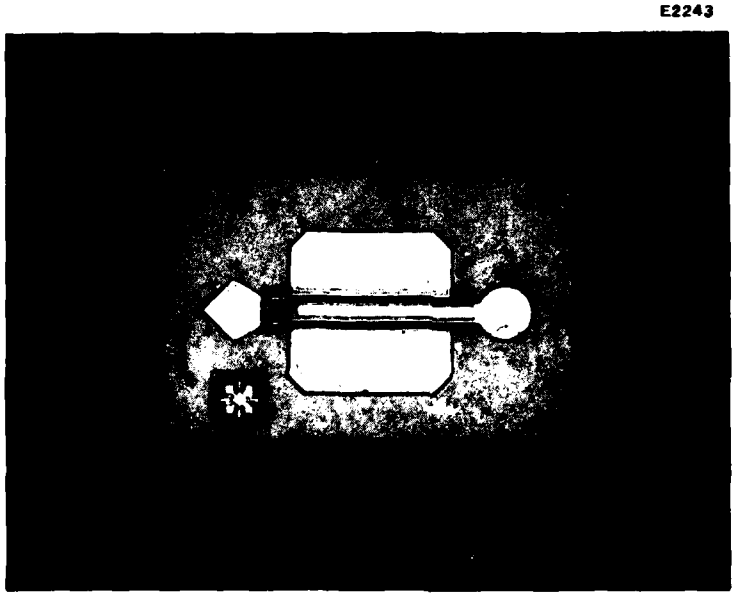


Figure 2-1 Optical photograph of FET A-10.

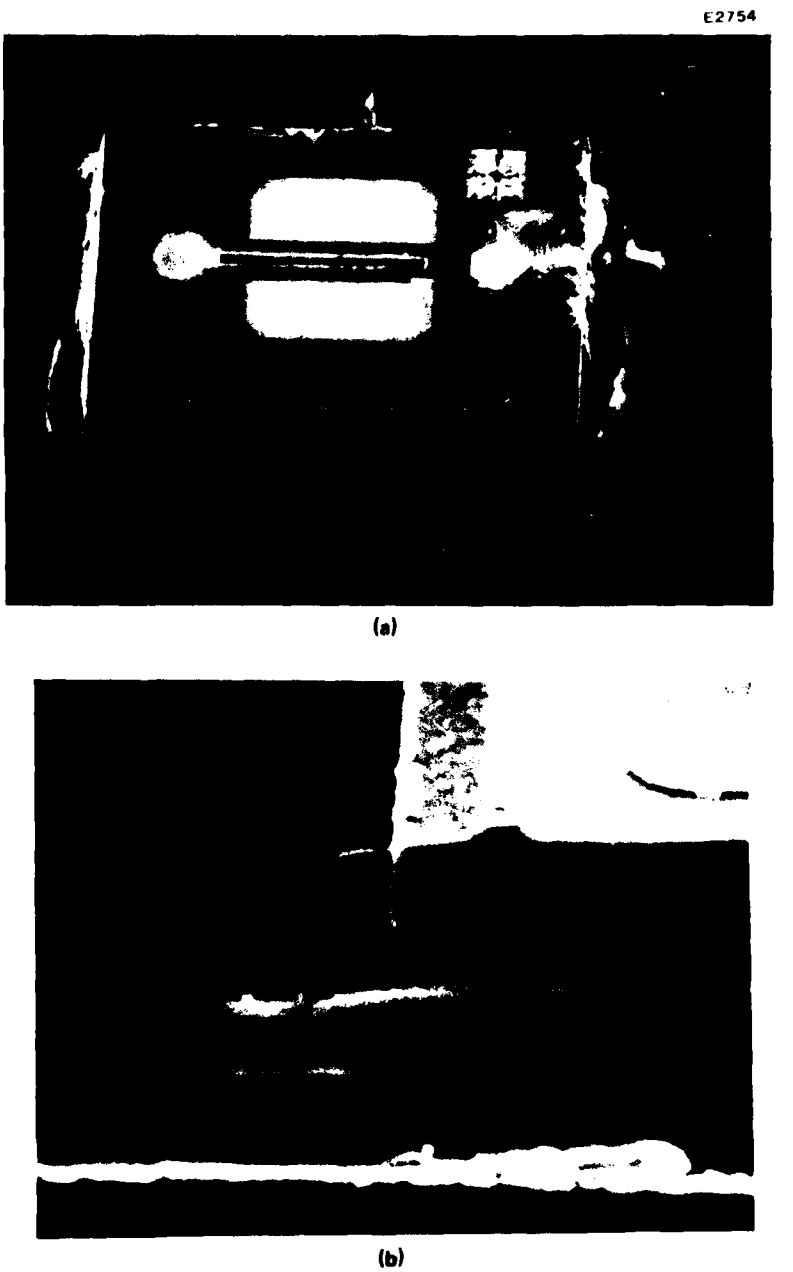


Figure 2-2 FET A-10. (a) Overall view, 196X, Glass intact. (b) Gate finger end, glass intact, 5200X. Note ragged gate metal edge due to lift-off.

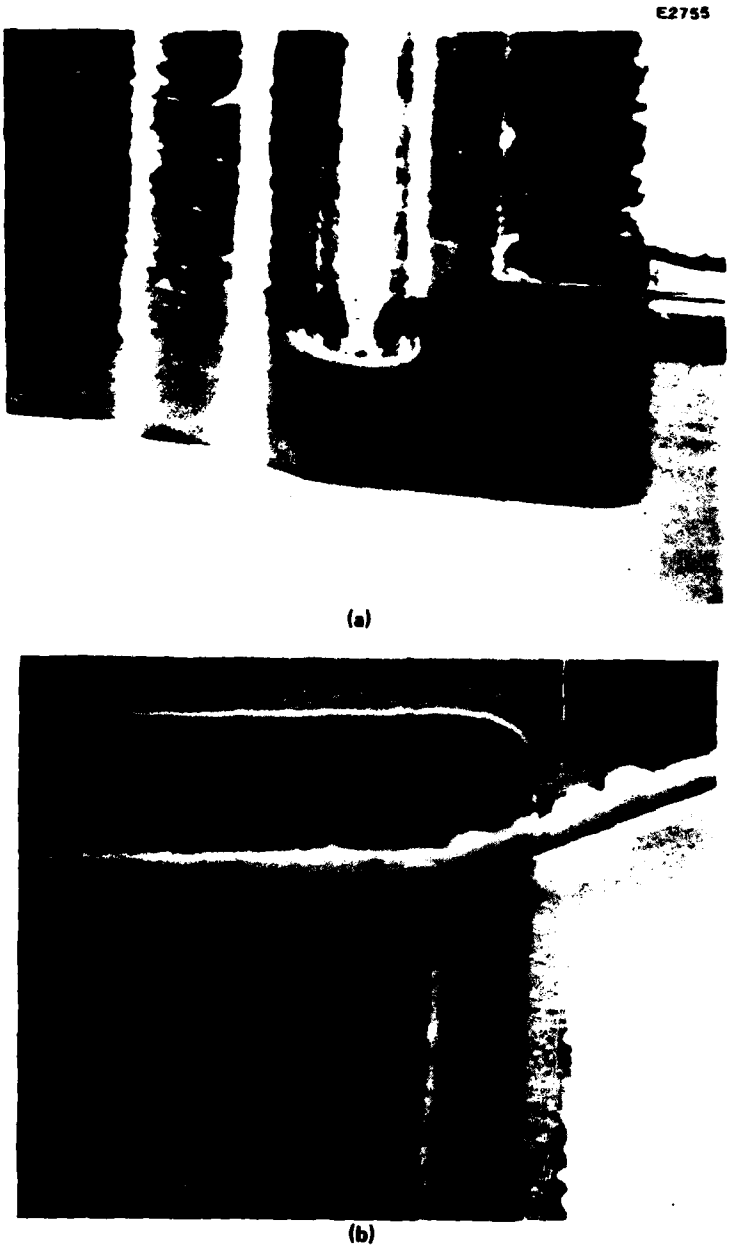


Figure 2-3 FET A-10. (a) Channel, glass partly removed, 5000X. (b) Gate pad, glass not etched, 5300X. Note ragged gate edge, Ti/Pt overlay, gold overlay to right.

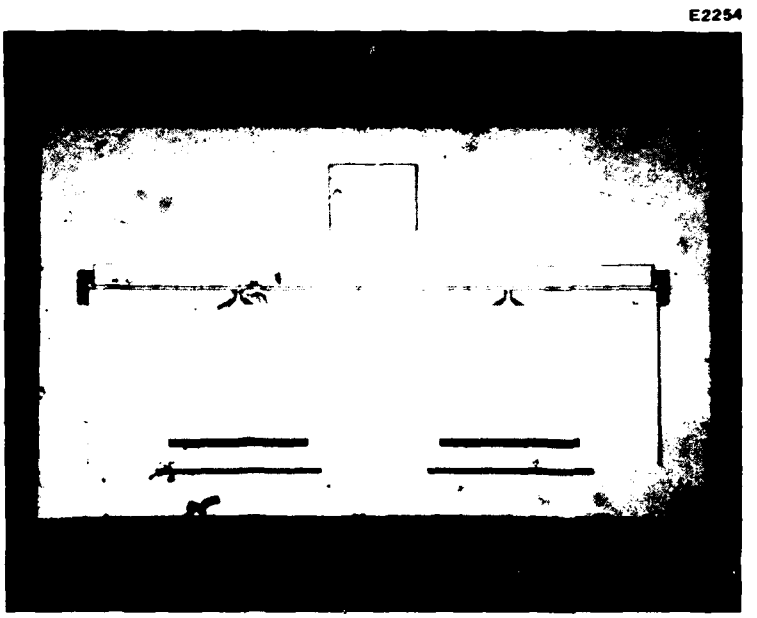


Figure 2-4 Optical photograph of FET D-1. The processing of this FET is basically identical to that of FET type D-2.

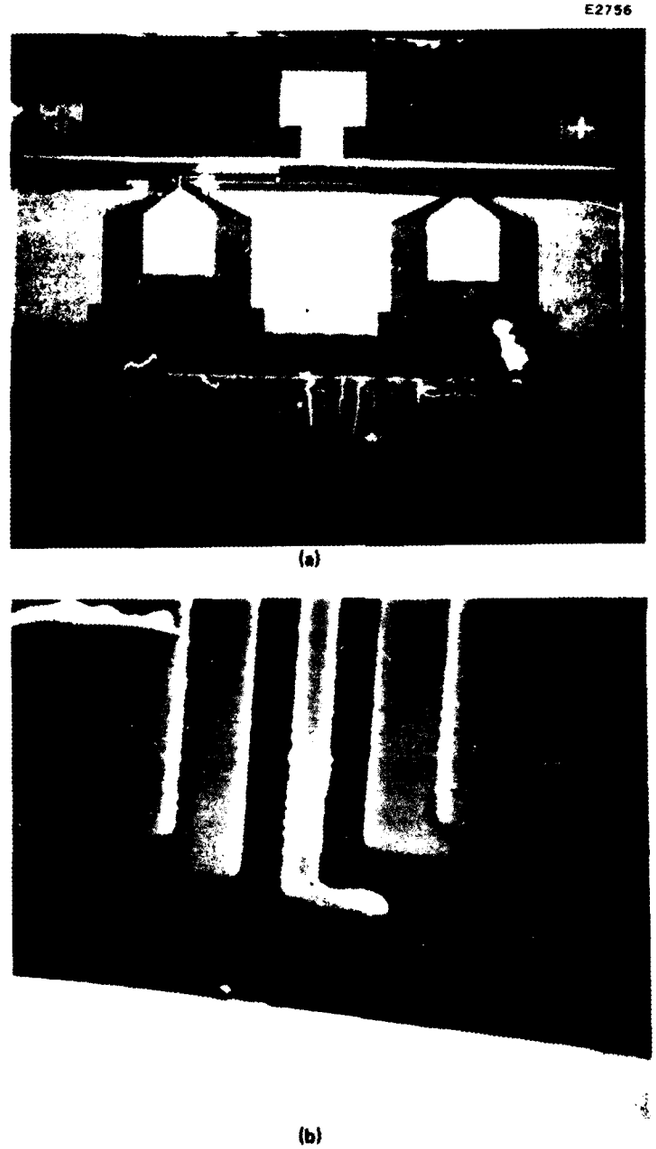


Figure 2-5 FET D-1. (a) Overall view, 196X. (b) Gate finger end, glass not etched, 4200X. Note interesting mesa step offset. Gate end crosses some shallow step as at pad connector.

E2255

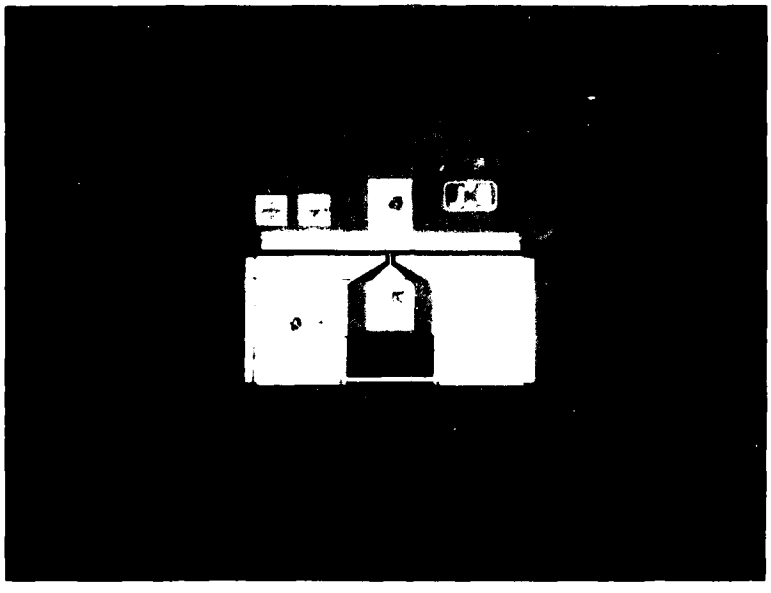


Figure 2-6 Optical photograph of FET D-2.

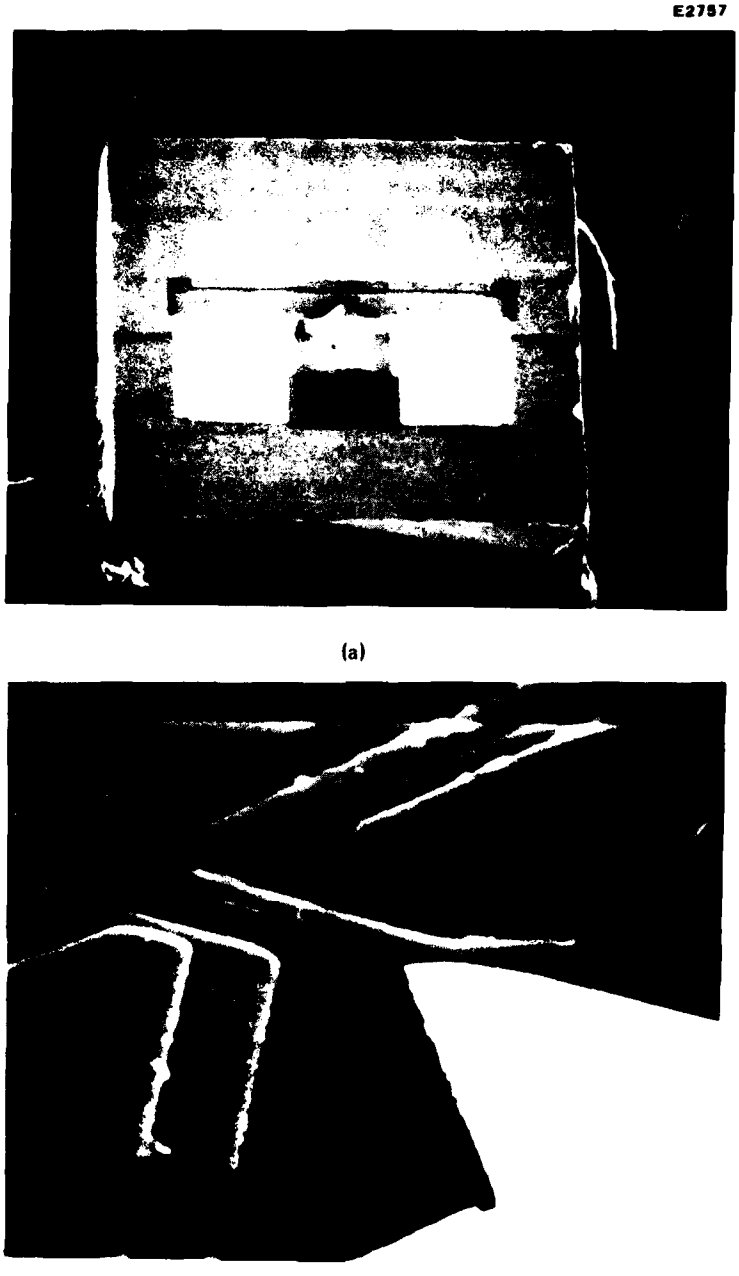


Figure 2-7 FET D-2. (a) Overall view, 190X with glass. (b) Gate connector, glass intact, at 5000X. Note (white) flake of glass missing from gate pad on right.

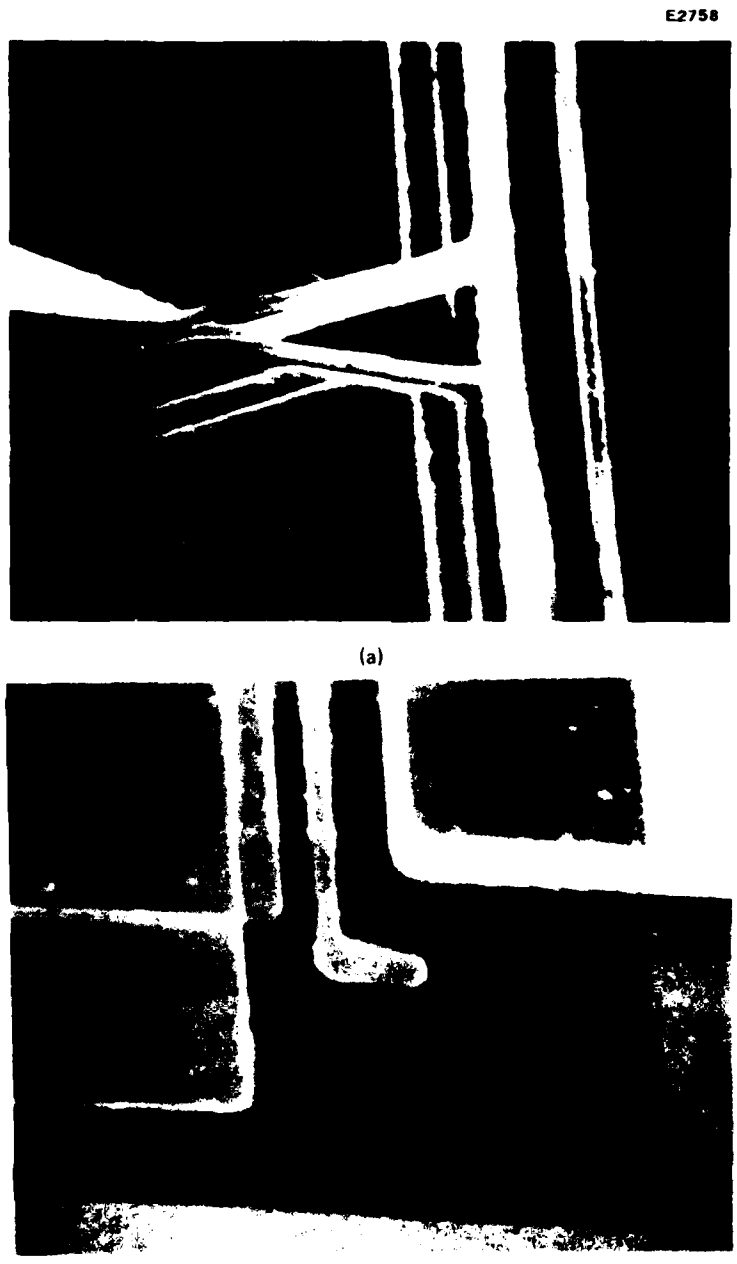


Figure 2-8 FET D-2. (a) 4400X view of gate metal after attempted removal of glass with buffered HF. Two layers are glass and gate metal. (b) Gate finger end, 4100X. Gate length, 0.8 μm; S-D spacing, 4.0 μm. Glass removed from ohmic contact.

Type H-1 (Figures 2-9, 2-10 and 2-11)

This device has an aluminum gate metallization. The gate is etched down into the channel and, as indiçated by the SEM photos prior to removal of the glass, was apparently formed by lift-off. In this device, as in the others, the aluminum gate was attacked during the process of removal of the glass. The gate is nearly in the center of the channel with a slight offest toward the source side. The gate pad is composed of a gold metallization over aluminum, and the EDAX scan does not show any other metals. However, we know that the gold is separated from the aluminum by a refractory layer. One unusual aspect is that the scan of the ohmic contact shows the presence of chromium as well as nickel. The device has a fairly sharp mesa step, but it is less than the thickness of the gate metallization. The gate stripe does not have an enlarged area at the ends and is also not constricted where it passes over the mesa edge. This uniformity at the mesa edge is probably a result of the use of a relatively shallow mesa etch.

Type N-2 (Figures 2-12 and 2-13)

This device shows similar construction techniques to that of the Type N-3 device, except that in the gate connector area the gold does overlay the aluminum for a short distance. It is also evident that the aluminum has been etched prior to deposition of the titanium, platinum, and gold. This device shows a sharp mesa step, as well as voids in the aluminum at the point where the gate stripe crosses over the mesa step. The mesa step appears to be about the same thickness as the aluminum.

Type N-3 (Figures 2-14 and 2-15)

The gate of this device is aluminum, and it is connected to a gold pad by a titanium/platinum overlay metallization. The gold does not overlay the aluminum. Scans of the ohmic contact show only platinum without any traces of the gold or germanium. This observation is probably an artifact of the EDAX measurement, as it is known that the gold-germanium alloyed contact is used for this process. The gate was largely destroyed in the process of removing the glass, and we were able to observe that there was no etching of the GaAs prior to the deposition of the gate. This construction

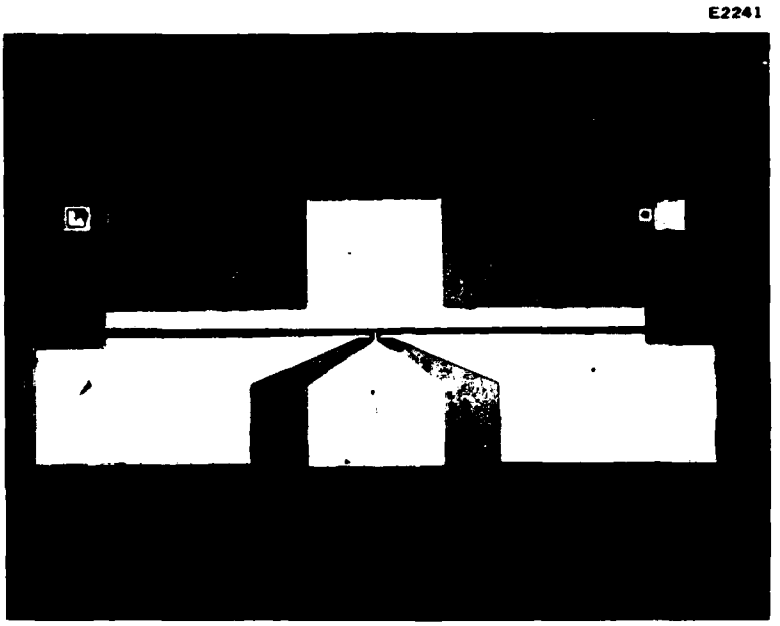


Figure 2-9 Optical photograph of FET Type H-1.

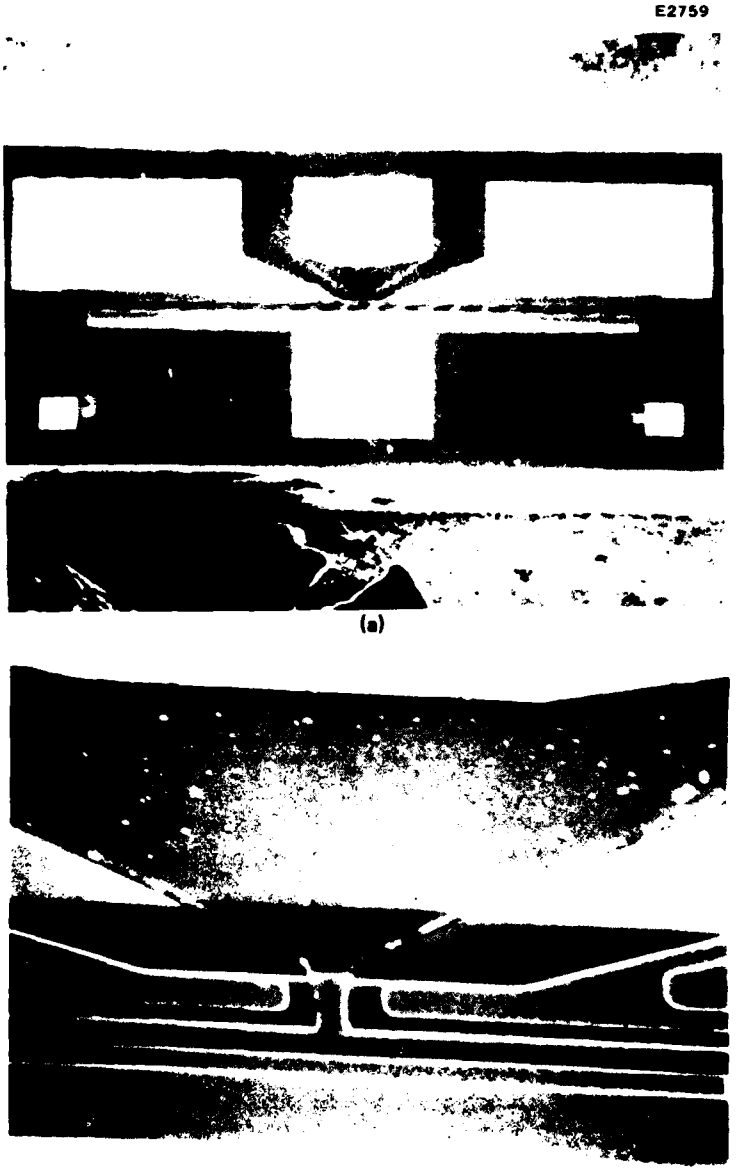


Figure 2-10 FET H-1. (a) Overall view with glass, 164X. (b) Gate connector, glass intact, at 1800X. Note ragged gate edges due to lift-off.

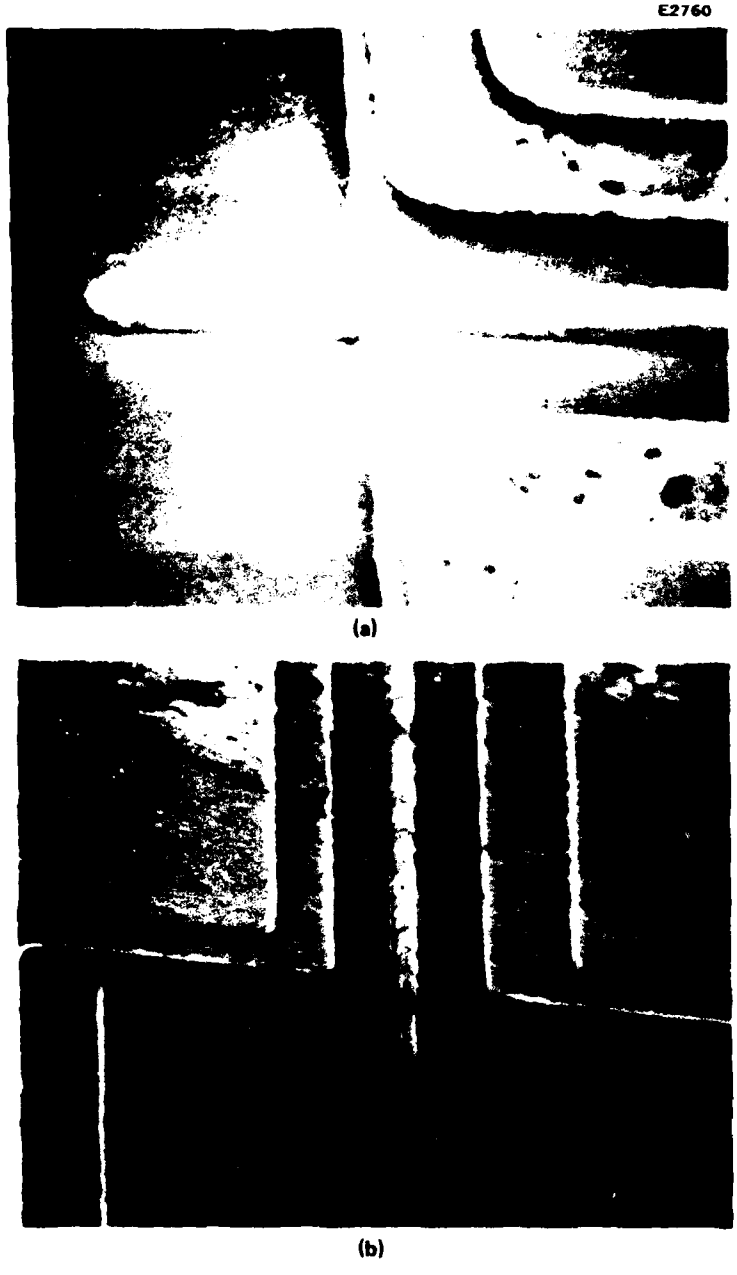


Figure 2-11 FET H-1. (a) Gate finger, 9000X, with glass. (b) Gate finger after buffered HF etch to remove glass, 4500X. Note etched channel under gate.

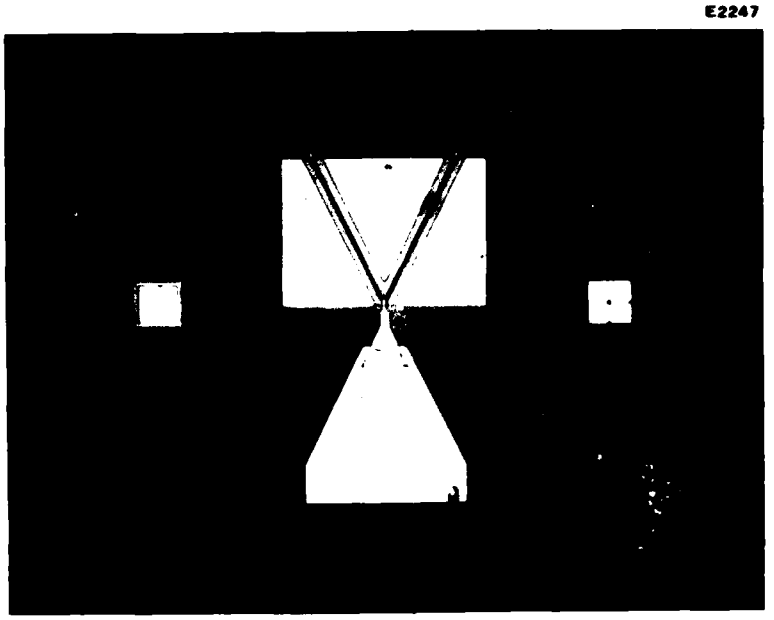
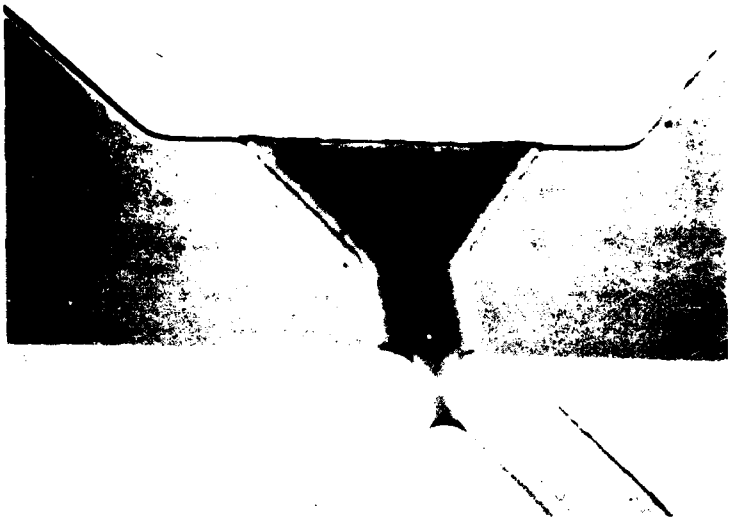
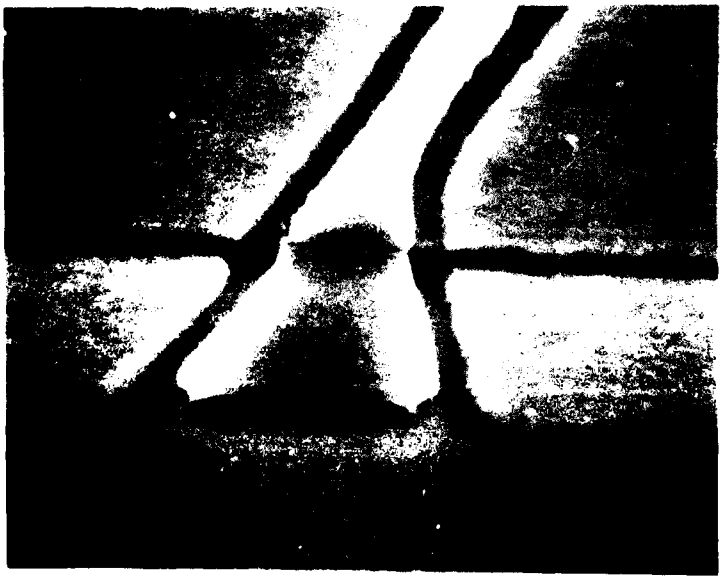


Figure 2-12 FET N-2. Optical photograph.

E2761



(a)



(b)

Figure 2-13 FET N-2. (a) Gate pad, 1800X, with glass intact. (b) Gate finger end, 9000X, glass not etched. Note slight undercut of gate metal. Effective gate length is 0.9-1.0 μm, S-D spacing 2.3 μm.

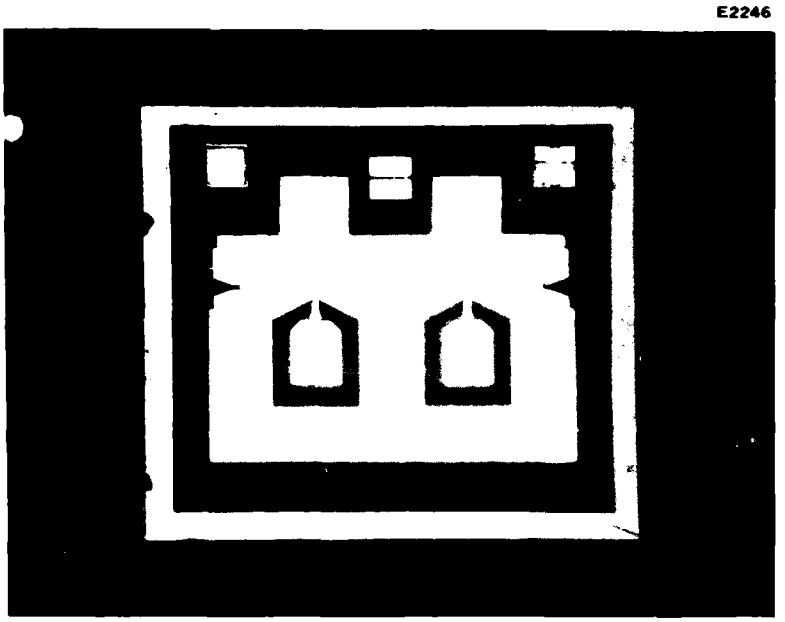


Figure 2-14 Optical photograph of FET N-3.

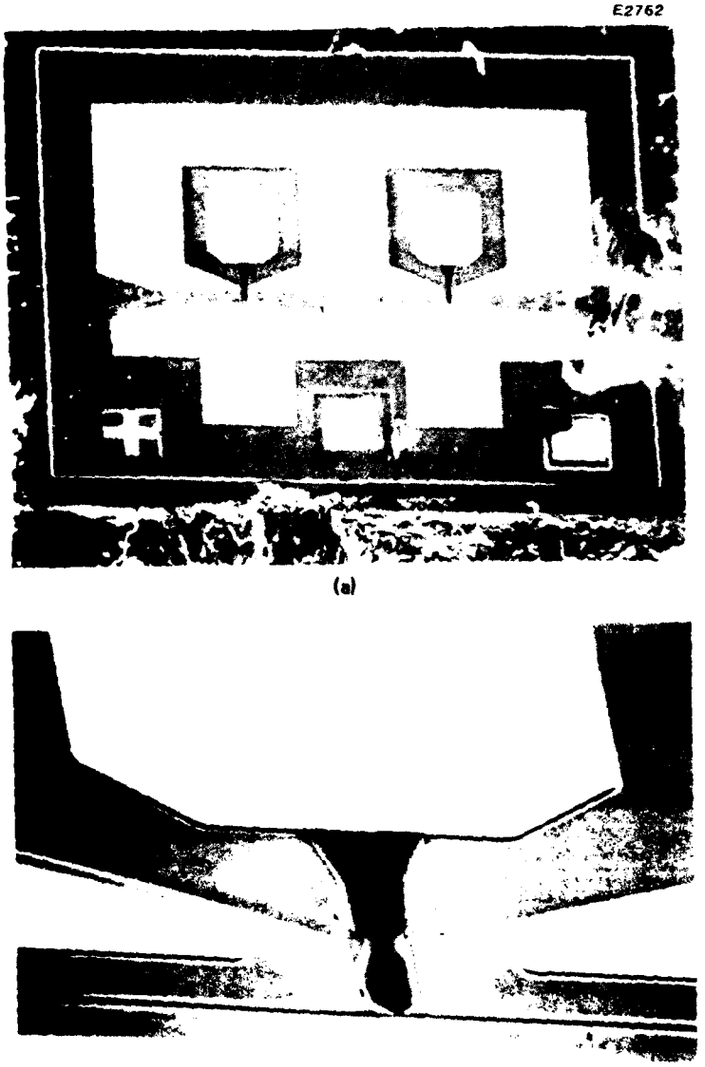


Figure 2-15 FET N-3. (a) Overall view, 220X, glass not etched. (b) Gate connector view, 1800X, glass not etched. S-D separation is 1.7 μm.

is in accord with the use of the self-aligned process. However, a photograph of the gate electrode taken prior to removal of the glass clearly shows that the gate is not in contact with the GaAs as it crosses over the mesa step and is considerably narrowed there. The gate also shows evidence of some etching prior to deposition of the titanium/platinum overlay connector.

Type P-4 (Figures 2-16, 2-17 and 2-18)

The gate metallization is aluminum and has been etched down into the channel. In addition, the ohmic contact metallization has also been etched down into a channel. The edge acuity on the gate is not particularly good, and the thickness of the gate electrode is less than half the gate length. Also, the gate etching appears to have been carried out on the [110] direction, such that the gate channel walls are vertical if not slightly undercut. This leads to spaces around the gate metallization that together at least equal the gate metallization length. In addition, the depth of gate etching is apparently about equal to the thickness of the gate metallization. There appears to be no overlay over the ohmic contact metal. The mesa step is sloping, and there is good coverage of the gate over the mesa edge. Obviously, the crystal directions were chosen to provide the sloping mesa edge, and this choice results in the undercutting of the gate etch.

Type P-5 (Figures 2-19 and 2-20)

The construction of this transistor is virtually identical to that of the P-4 device. In the SEM photos there are some clear views of the gate not crossing over the mesa, due to incomplete exposure of the photo resist, and very nicely formed undercut walls of the etched channel. In this particular case, the depth of channel etching is perhaps nearly twice the thickness of the gate metallization, which is very deep for a low noise device. Scans of the ohmic contact metal on this device, as well as on the P-4 device, show no evidence of anything other than gold. Gate metallization is aluminum, probably formed by liftoff.

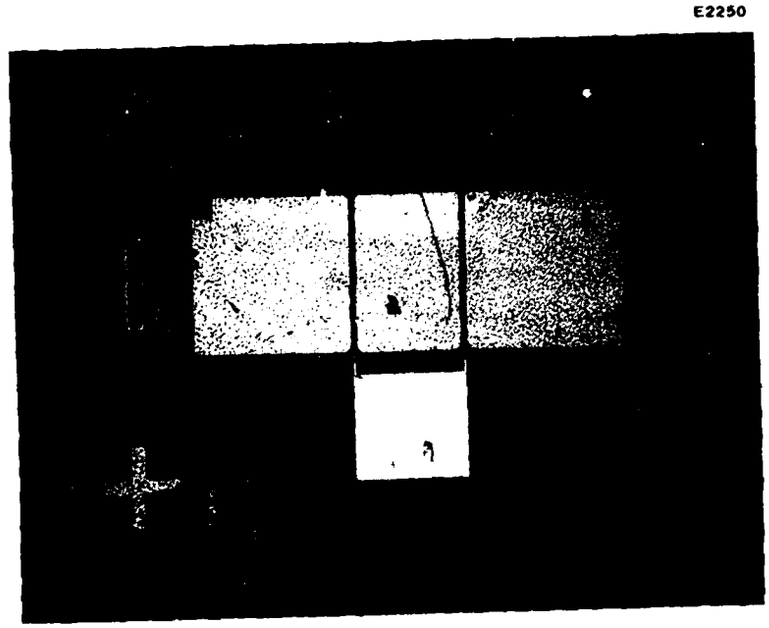
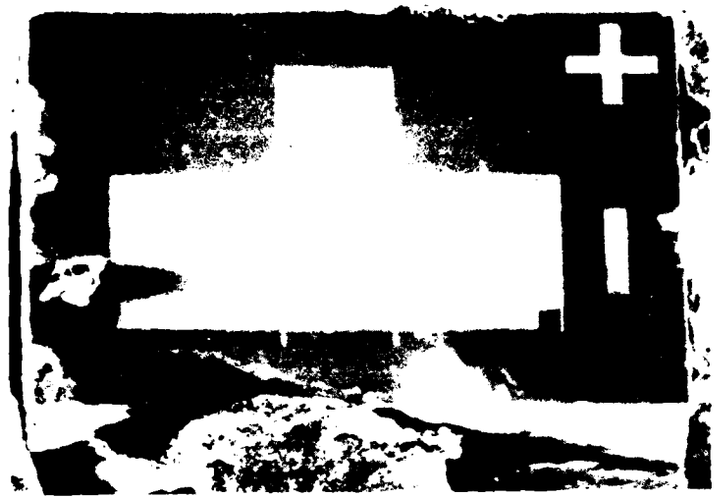
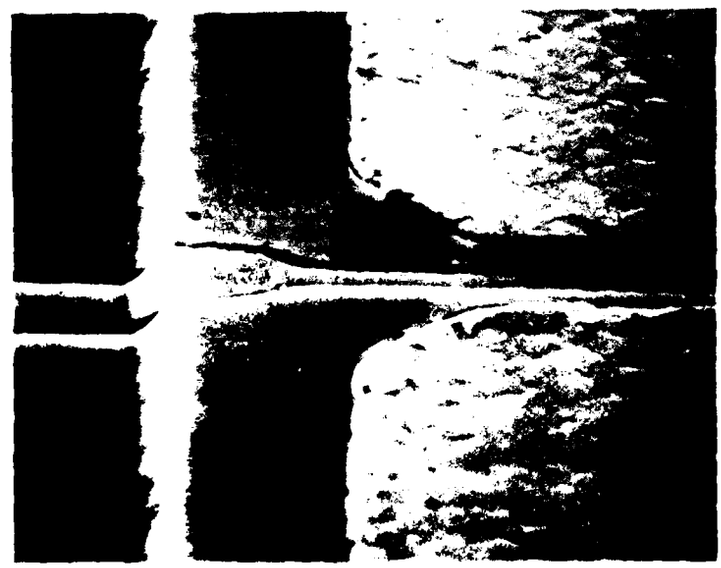


Figure 2-16 Optical photograph of FET P-4.

E2763



(a)



(b)

Figure 2-17 FET P-4. (a) Overall view, 162X. Device has no glass as received. (b) Gate connector, showing very deep recess. Note beveled mesa edge.

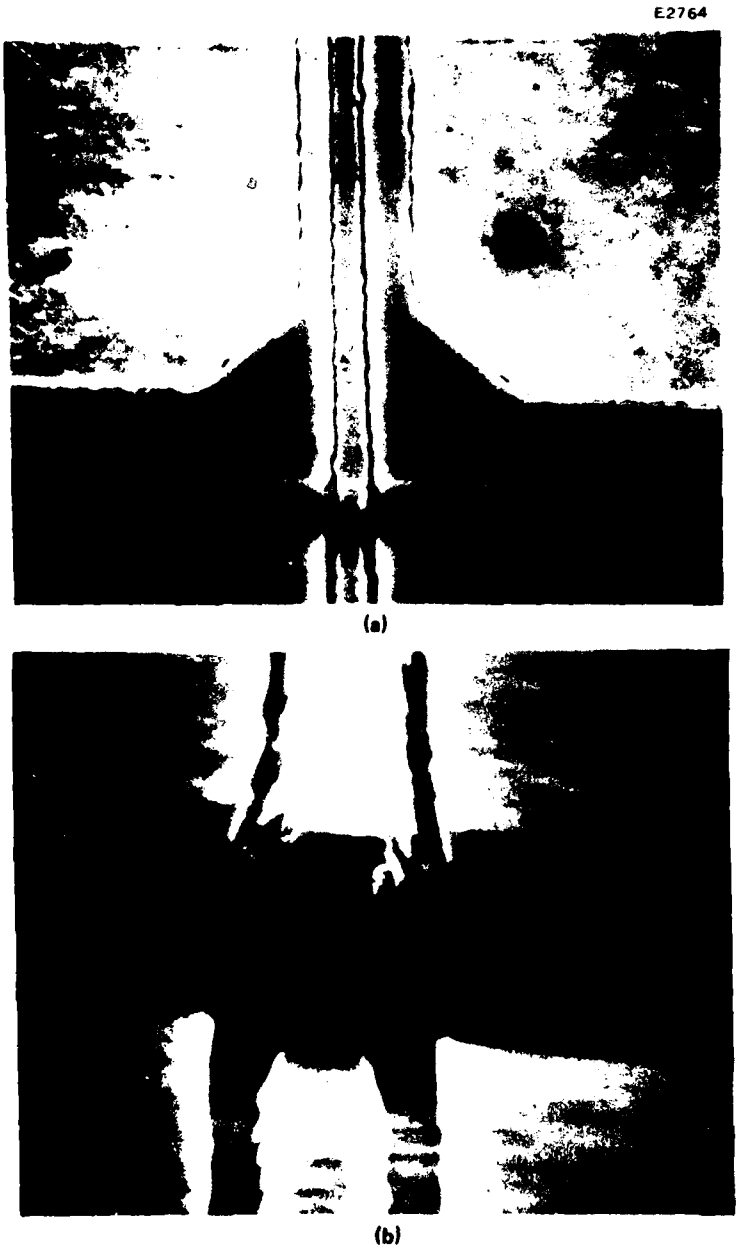


Figure 2-18 FET P-4. (a) End of channel, 4200X. Note recessed S-D ohmic contact. S-D spacing is 4.0 μm. (b) Gate finger end over mesa edge, 18,000X. Note undercut of gate channel, indicating use of preferential etch. Gate length, 1.1 μm; thickness, 2800Å.

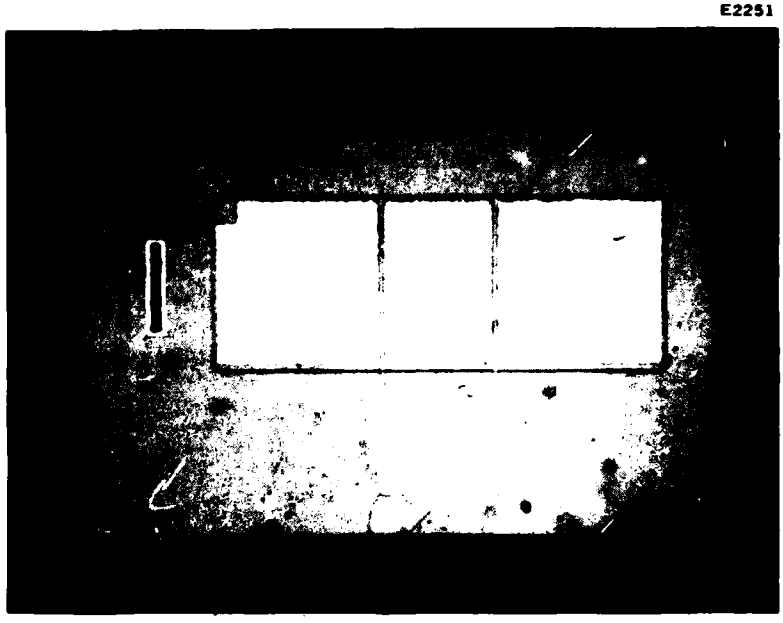


Figure 2-19 FET P-5. Optical photograph. This device is identical in geometry and basic construction to the P-4.

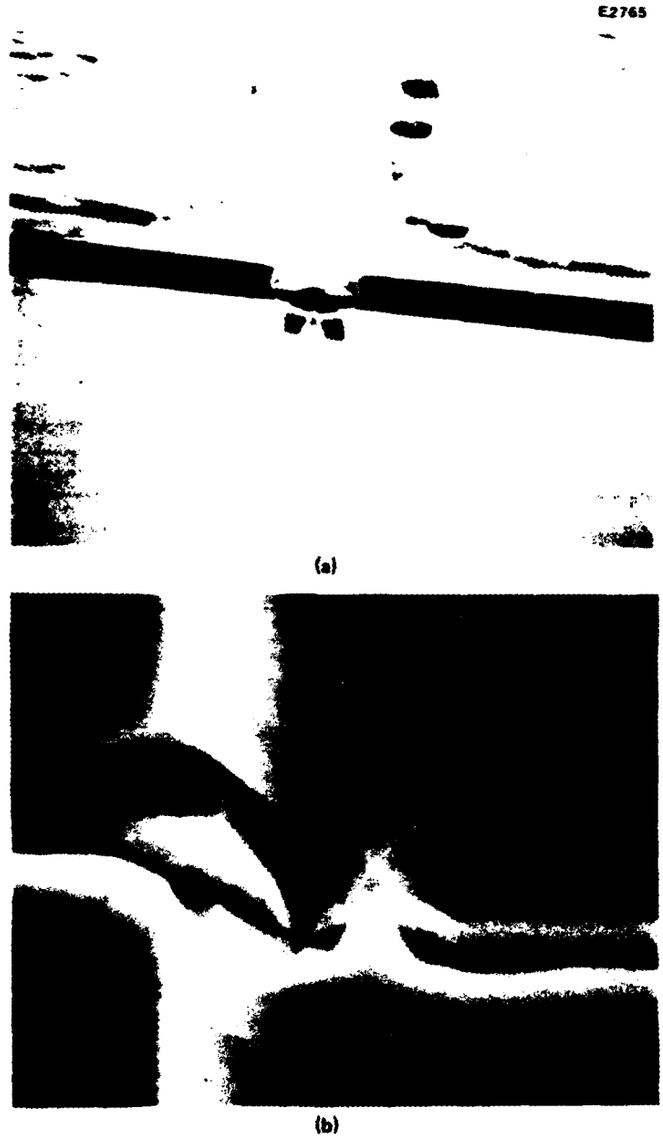


Figure 2-20 FET P-5. (a) Gate finger end, 4500X, showing ragged and recessed S-D metal and recessed gate. S-D spacing, 4.9 μm. Gate length, 0.9 μm. (b) Resist defect at end of gate finger. Evaporant arrived from left, shadowing the profile. Gate etch depth, 1.3 μm; 2800Å of Al.

Type R-2 (Figures 2-21, 2-22 and 2-23)

On this device we have an EDAX scan of the gate showing that it is aluminum. The topography of the device shows that the gold metallization, because of the choice of mask geometry, overlaps onto the aluminum. The gate is obviously formed by liftoff and has a relatively fine grain. It is also recessed into the channel by a slight etch, which is perhaps 1/3 of the thickness of the gate metallization. Detailed pictures of the gate connector metallization show a number of what appear to be separations between the transition and the gate metallization. Pt was found by EDAX in the area where a refractory barrier layer should be between the Al gate and Au pad. The mesa step is cut in two steps so that there is a series of steps for the gate connector, but in the region where the gate runs over the end of the mesa there appears to be only one step, which is perhaps three times the height of the gate metallization. The gold metallization over the ohmic contact appears to be quite thick as well and is probably formed by ion etching, judging from the geometry of the edges. The channel has been etched to the edges of the S-D metal, probably by ion etching or sputtering prior to deposition of the gate electrode. This ion etching process may also be responsible for some of the breaks seen in the gate connector metallization, as it is known that preferential etching of a surface in the vicinity of an adjacent side wall occurs due to ricochet of the sputtered atoms. Figure 2-23(b) clearly shows complete separation of the gate metallization from the connector.

Type R-5 (Figures 2-24, 2-25 and 2-26)

This device has a gold-refractory gate metallization, and the EDAX scan also shows the presence of chromium. The gate geometry is quite regular and well defined and is recessed into the channel by an amount that is nearly equal to half the gate thickness. The gate thickness is greater than half the gate length. In this device also, the ohmic contact metallization has been recessed into the epitaxial layer. The device had no glass coating.

E2245

Figure 2-21 Type R-2 FET, optical photograph.

Figure 2-22 Type R-2 FET. (a) Overall view, 88X, glass intact. Arrow shows view of Figure 2-23(b). (b) Gate pad area. Light area at top is gate pad opening in the glass. 860X, glass intact. Note gray refractory metal band just below gold gate pad.

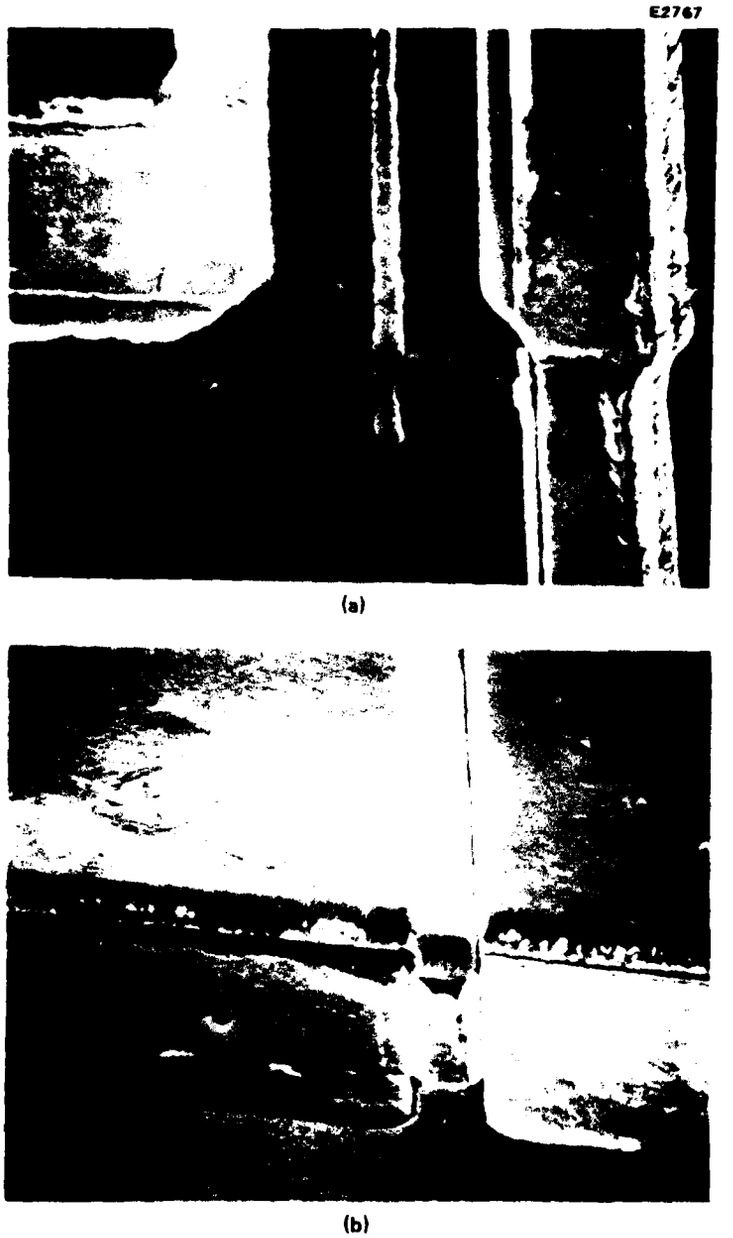


Figure 2-23 Type R-2 FET. (a) Glass removed, 4200X. Gate length, 1.4 μm; S-D separation, 7.3 μm. Note channel etch around gate and GaAs etching at S-D edges. (b) Glass etched off, 4400X. Detail of gate pad connector. Gate to left. Note separated pad over step. Refractory metal band is visible, lower left.

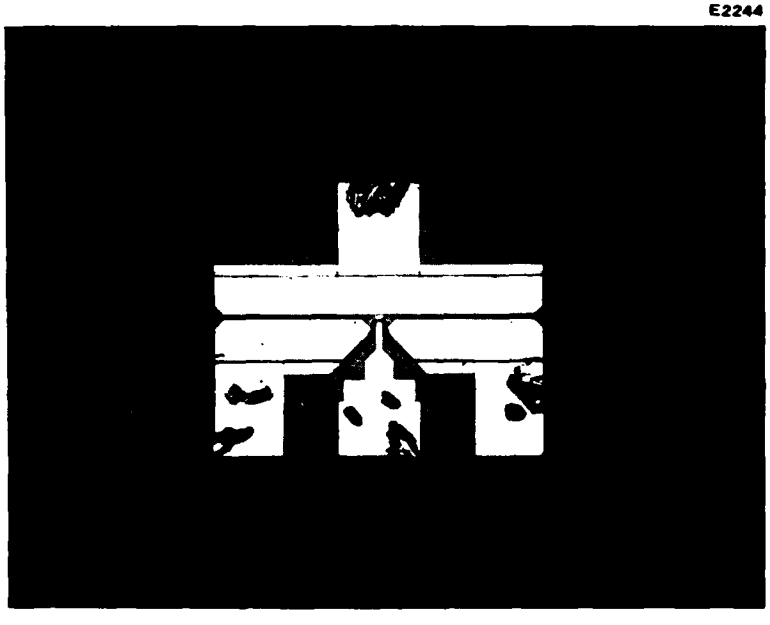


Figure 2-24 Optical photograph of .Type R-5 FET.

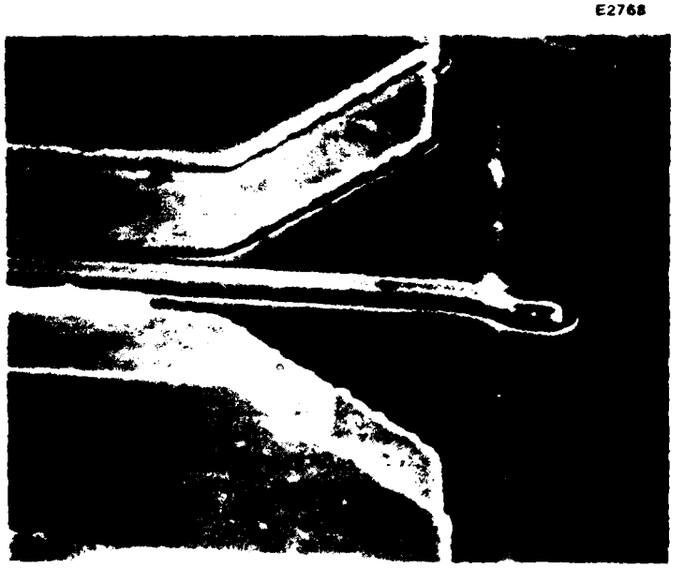


Figure 2-25 SEM photograph of FET R-5 at 4300X. Note the white fringe of metal on the source electrode (left-bottom of picture), indicating poor lift-off. Note recessed gate and source/drain electrodes. Gate length is 1.1 μm, S-D separation is 4.4 μm.

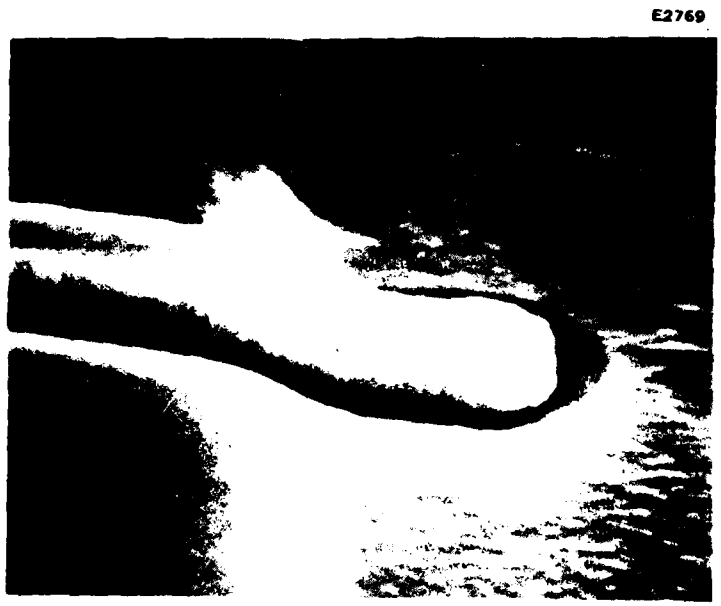


Figure 2-26 SEM photograph of gate finger end, FET R-5 at 18,000X. Estimate 500-1000Å of CR, overlaid by 4500-5000Å of Au.

The gate edges are quite steep and sharp, and the gate is centered in the etched channel. This centering could only have been done by a self-aligned process, so it can be concluded that the gate was achieved by liftoff. The process was well done, however, because the gate edges show no evidence of any shearing of metal during the lifting process. Interestingly, the EDAX scan shows evidence of chromium and nickel in deep probing of the source and drain pads.

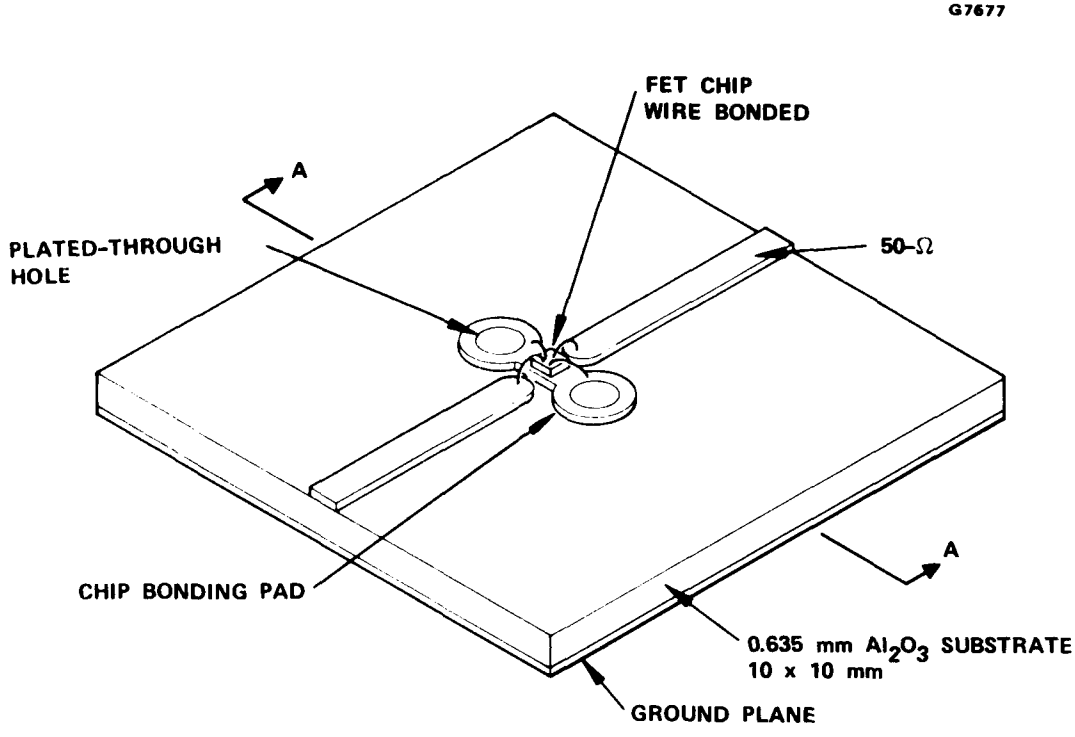
Summary

The SEM/EDAX examinations revealed much about the processes and materials used in these devices. However, only limited data could be obtained concerning composition of thin refractory metals under thick gold layers. In some cases a gallium etch developed by Hughes on another RADC program was used to remove the gold metal, thereby exposing the underlying refractory metallization for SEM/EDAX examination. See Section 3.4 of the Final Report, "Failure Mechanism Study of GaAs FET Technology," Contract F30602-78-C-0326.[1] The EDAX measurements, as expected, did not reveal the composition of the glass overlayers.

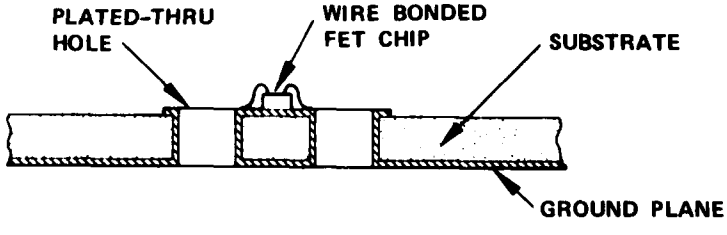
2.4 DC MEASUREMENTS

All test samples used for this investigation were measured (generally with a Tektronix 576 Curve Tracer) to determine their important DC characteristics. Most were also measured for RF characteristics near 10 GHz and for S-parameters over the 2-12 GHz frequency range, as discussed in succeeding sections. The several DC characterization procedures that generally were used are described below.

Before being tested, each FET chip sample was permanently mounted on a 1 cm^2 alumina microstrip carrier (Figure 2-27) using Au-Sn eutectic and gold wire bonds. These carriers provide a safe and convenient means of handling and testing the devices. The microstrip is a good medium for both DC and microwave characterization of the FET, and the life test ovens are designed to use the carriers for applying DC bias to the FETs.



(a) Top view



(b) Cross section through center perpendicular to microstrip lines.

Figure 2-27 One cm^2 microstrip chip carrier.

During DC testing the carriers are clamped in a microwave test fixture with X-band bias tees and are terminated by a 50 ohm load. The bias circuits described in Section 5-1 are connected to the bias tee DC ports. The FETs were always tested and operated with the source grounded. Full DC characterization was done before stress testing began and periodically during testing.

Figure 2-28 shows a typical set of GaAs FET current-voltage (I-V) curves, as seen on a curve tracer with the FET connected in the common source configuration. The primary DC characteristics that are generally important to low-noise operation and our standard measurement conditions are summarized below.

- Specific Drain Current

  I_{DS}: I_D for $V_D = 0.5$ V, $V_G = 0$

  The specific drain current is measured in the linear portion of the I-V curves and is a useful measure of source-drain parasitic resistance.

- Saturated Drain Current

  I_{DSS}: I_D for $V_D = 1.5$ V, $V_G = 0$

  Although the data in Table 2-2 indicate that I_{DSS} is typically measured at a drain voltage of 3 volts or more, when we made measurements on the curve tracer we found that the devices tended to oscillate unless we reduced the drain voltage below 3 volts. To assure a consistent, stable set of DC measurements we standardized on making all I_{DSS} measurements at a drain voltage of 1.5 V.

- Low-Noise Transconductance

  g_m: $\Delta I_D / \Delta V_G$ at $V_D = 1.5$ V, V_G from -0.5 V to -1.0 V

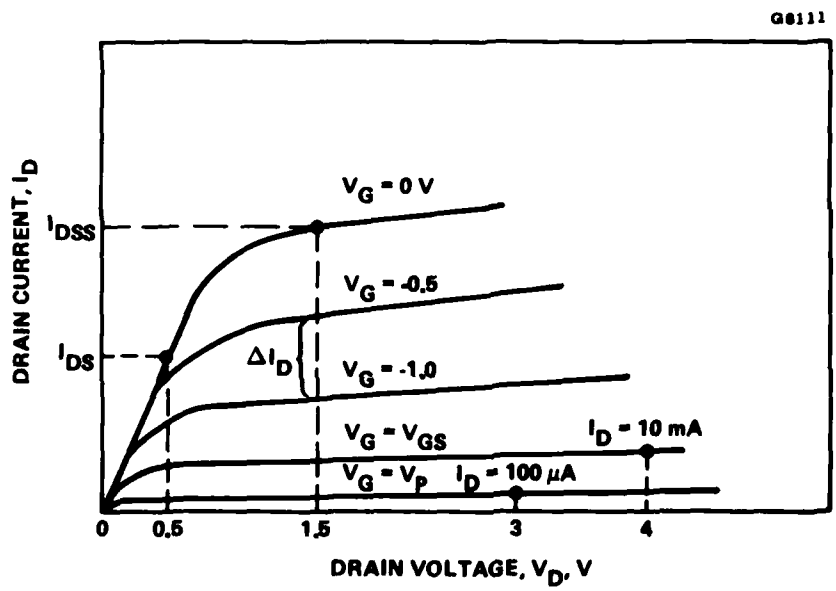


Figure 2-28 Typical GaAs FET I-V curves for the grounded source configuration.

This is a measure of the gain of the transistor in the neighborhood of the maximum RF gain point.

- Low-Noise Gate Bias

$$V_{GS}: V_G \text{ for } V_D = 4\ V, I_D = 10\ mA$$

Optimum low-noise operation is typically somewhere in the neighborhood of this bias point. V_{GS} was always measured at the oven temperature. The other DC parameters were always measured at room temperature.

- Gate Pinchoff Voltage

$$V_P: V_G \text{ for } V_D = 3\ V, I_D = 100\ \mu A$$

This is a convenient measure of the gate bias necessary to fully deplete the intrinsic source-drain channel of free majority carriers.

Besides the five DC parameters discussed above, we monitored the reverse breakdown voltage characteristic of the Schottky-barrier gate. Our procedure was to short the drain to the grounded source and then to monitor the gate current I_G as reverse bias voltage was applied to the gate. Typically, we would record the reverse gate voltage that resulted in -3 μA gate current, provided the gate voltage did not exceed -10 volts. In some cases, in order to obtain measurable current, the reverse gate voltage was allowed to exceed the manufacturer's recommendations, but only if the magnitude of the gate current remained small (less than 3 to 4 μA). Usually, over time the gate diode reverse characteristic remained substantially unchanged, unless the gate diode failed, in which case the reverse gate current increased an order of magnitude or more.

In addition to these specific parameter measurements, a photographic record of the full family of I-V curves was made.

Typical initial measurements of DC parameters for the low noise FET devices are given in Table 2-4. Manufacturer's specifications for the parameters were presented in Table 2-2.

TABLE 2-4

TYPICAL INITIAL MEASUREMENTS OF DC PARAMETERS
FOR THE LOW NOISE FET DEVICES

Type Code	I_{DS}, mA	I_{DSS}, mA	(See Note) V_{GS}, V	V_p, V	g_m, mmho
A-10	22	43	-4.0	-2.50	32
A-6	29	45	-1.2	-1.75	28
D-1	25	47	-3.0	-2.50	35
D-2	17	37	-1.3	-2.00	28
H-1	27	51	-1.5	-1.70	46
H-11	26	48	-1.7	-2.10	40
N-3	20	42	-2.5	-1.75	30
P-5	40	70	-2.2	-4.50	30

Note: Measurements were made at room temperature for all parameters except V_{GS}. V_{GS} measurements were made on the FETs in the oven at the stress temperature.

2.5 RF TESTS

In addition to DC measurements, RF measurements were made near 10 GHz on most devices. Measured parameters included minimum noise figure and associated gain, maximum available gain, and power out and gain at 1 dB gain compression. The S-parameter measurements are discussed in the following section. After the initial characterization, RF and S-parameter measurements on devices undergoing temperature stress testing were taken on about 20% of the devices, with full characterization again following the end of the tests.

For the noise figure, power, and gain measurements, the manufacturer's recommendations we followed in setting the DC bias conditions. For uniformity in the RF tests we used a frequency of 10 GHz (sometimes 10.05 GHz to avoid RF interference from a 10 GHz TWT in the laboratory), although the manufacturer may not specifically have recommended operation at 10 GHz. As a consequence of testing some devices at a frequency other than the manufacturer's suggested optimum frequency, absolute values of noise figure, power out, and gain may not be compared. We were able to observe, however, when parameter values changed. As the formal failure criteria (see Section 2.7) were specified in terms of changes in DC parameters, the RF and S-parameter data are useful mainly for corroborative purposes.

- Minimum Noise Figure and Associated Gain

  The minimum noise figure F_{min} and associated gain G_a were measured near 10 GHz following the manufacturer's recommendations for the DC bias conditions. These device characteristics were tracked not only because they are a direct indication of operational performance, but also to investigate the correlations between the aging characteristics of the DC and RF parameters. Measuring RF characteristics is considerably more expensive and time consuming than measuring DC characteristics; therefore, if significant correlations can be obtained, cost and time savings can be made by relying primarily on DC measurements, with RF measurements used only for spot checks and confirmation.

A schematic of the F_{min}-G_a measurement system is shown in Figure 2-29. The device under test (DUT) is mounted between two double-slug tuners. This combination forms a single-stage amplifier, which is manually tuned for minimum 10-GHz noise figure. The calibrated noise source and precision noise figure meter are connected to the amplifier input and output ports, respectively, for this purpose. The associated gain of the amplifier is measured by switching its input to the 10 GHz sweep oscillator signal and its output to the microwave power meter. The measured noise figure F_{meas} and associated gain G_a are then used to calculate the minimum noise figure F_{min} of the FET:

$$F_{min} = F_{meas} - \frac{F_o - 1}{G_a},$$

where F_o is the measured noise figure of the output circuitry, consisting of the output bias tee, isolator, switch, mixer, IF amplifiers, etc. No correction was attempted for the losses of the double-slug tuners.

A comment is in order concerning the measurement accuracy of the F_{min}-G_a measurements. Table 2-5 summarizes the results of F_{min}-G_a measurements on accelerated-life-test control FETs that were carried out on a previous RADC program.[2] The RF failure criteria adopted for these life tests were F_{min} = +0.5 dB and G_a = -1.0 dB. The combined RF measurement errors (standard deviations), as shown at the bottom of Table 2-5, are thus 26% and 32%, respectively, of these limits. At least two factors contributed to these relatively large measurement errors. First, the SMA coaxial connectors used in the measurement system were sensitive to mechanical stresses and could have relatively poor repeatability. Second, tuning of the input and output double-slug tuners is subject to operator error. To improve the accuracy and ease of making RF measurements, during the course of the program we converted our RF test setup to use APC-7/microstrip connectors and 7 mm slab-line tuners, which have lower loss and better reproducibility than SMA coaxial connectors.

Because of the difficulty and cost of making noise figure and gain measurements, some investigators have used fixed-tuned single-stage amplifiers for RF measurements. Although this procedure significantly reduces measurement error and the operator time

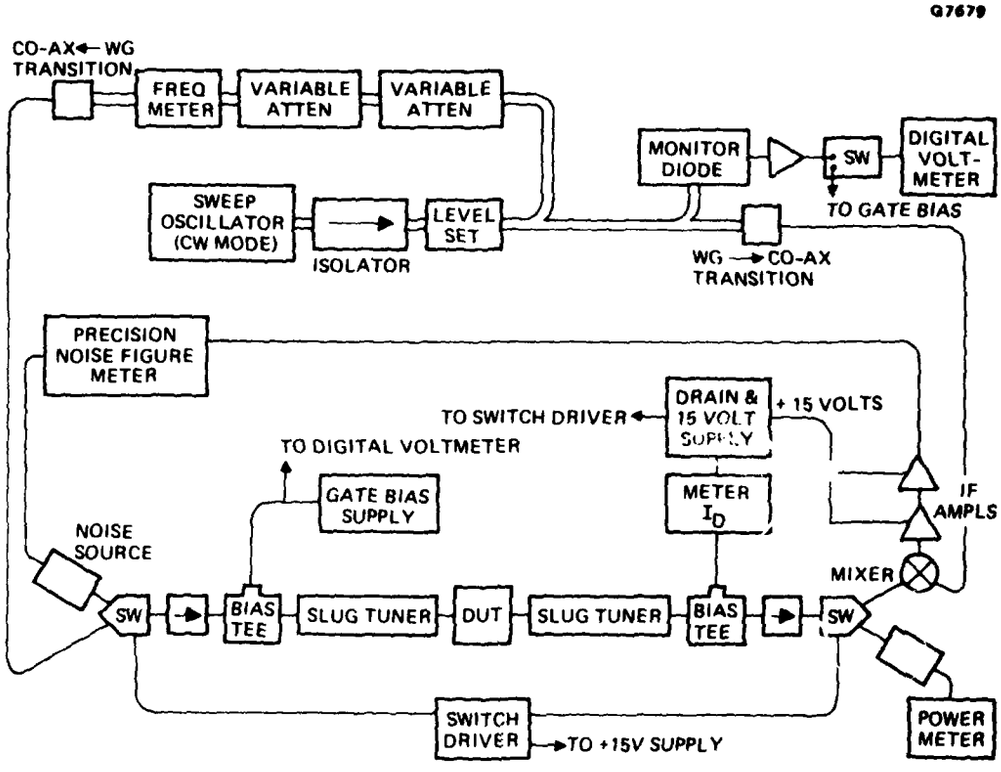


Figure 2-29 10-GHz noise figure and gain measurement system.

TABLE 2-5

SUMMARY OF RF MEASUREMENTS ON CONTROL FETs FROM A PREVIOUS RADC RELIABILITY PROGRAM (2)

FET Type	Control FET No.	Number of Times Measured	Average Value (Standard Deviation)	
			F_{min}, dB	G_a, dB
A2	A2-C1	18	3.097 (0.127)	5.990 (0.309)
	-C2	12	3.070 (0.122)	6.132 (0.361)
	-C3	14	3.381 (0.169)	6.006 (0.313)
B	B-C1	8	3.119 (0.122)	6.659 (0.219)
	-C2	6	3.332 (0.140)	7.400 (0.491)
	-C3	8	3.086 (0.082)	7.000 (0.256)
C	C-C1	9	3.623 (0.112)	6.499 (0.406)
	-C2	6	3.455 (0.194)	7.103 (0.340)
	-C3	8	3.466 (0.124)	6.793 (0.380)
All	All	89	(0.129)	(0.324)

required, extracting the actual device RF characteristics from the overall circuit characteristics is difficult. We have chosen to tune the FETs individually.

- Maximum Available Gain

  The test setup of Figure 2-29 was tuned for maximum gain G_{max} using the manufacturer's recommended settings for DC parameters, with zero voltage on the gate. The frequency was near 10 GHz.

- RF Power Output and Gain at 1 dB Gain Compression

  The drain voltage was set the same as for the I_{DSS} measurement. The negative gate voltage was then adjusted until the drain current was 0.5 I_{DSS}. As the RF drive level near 10 GHz was increased from zero, the RF power output and gain were monitored until the gain decreased 1 dB. The RF output power at this point was recorded as $P_{-1\ dB}$.

  Typical initial measurements of RF parameters at 10 GHz for the low noise FET devices are given in Table 2-6. Manufacturer' specifications for the parameters were presented in Table 2-2.

2.6 S-PARAMETERS

Scattering parameter (S-parameter) measurements were made on the low noise FET chips and packaged devices using one of two automatic network analyzer (ANA) systems. Early measurements in the program were made on the somewhat limited facilities of another Hughes division. Later measurements were made in our own laboratory at the Hughes Torrance Research Center using the Hewlett-Packard 8542B ANA system. This facility has the capability for limited de-imbedding of the FET device S-parameters from the overall measurements and can also make Smith chart plots automatically over the frequency range for each S-parameter. We have also been working on internally-funded programs to improve the accuracy and reproducibility of S-parameter measurements with the 1 cm^2 microstrip carrier shown in Figure 2-27. Throughout the changes and modifications, care has been taken to assure continuity of the test results as much as possible.

TABLE 2-6

TYPICAL INITIAL MEASUREMENTS OF RF PARAMETERS AT 10 GHz
FOR THE LOW NOISE FET DEVICES

Type Code	F_{min}, dB	G_a, dB	G_{max}, dB	P_{-1dB}, dBm
A-10	4.0	6.4	10	+4
A-6	2.7	7.7	10	+10
D-1	6.0	5.1	6	+2
D-2	4.6	8.0	9	+4
H-1	3.9	5.0	10	+13
H-11	3.8	5.4	9.5	+9
N-21	5.4	6.0	10	+5
N-3	3.6	6.2	7.2	+7
N-31	3.4	9.5	13.6	+9
N-32	5.2	7.4	8.3	+8
P-5	3.0	5.4	7.9	+7

Note: These measurements were made at 10 GHz, using DC bias conditions suggested by the manufacturer for optimum performance not necessarily at 10 GHz, as shown in Table 2-2.

The HP 8542B automatic network analyzer is capable of making detailed scattering-parameter measurements to 18 GHz. However, results are limited to 12 GHz because of parasitic effects in the carrier. The S-parameter data were taken in 200 MHz steps from 2 to 12 GHz and are stored on magnetic disk to be retrieved at any time.

The ANA configuration is standard and will not be described here. The measured S-parameters can be used to calculate the impedance or admittance characteristics of the FET. The data can also be used to calculate the maximum available gain, maximum stable gain, etc., of the device as a function of frequency. Because for this study we were interested in low-noise operation of the tested GaAs FETs, all S-parameter measurements were made with DC bias set at V_{DS} = 3.5 V and I_{DS} = 10 mA.

Most devices were given an initial S-parameter characterization, and devices surviving the stress testing programs were 100% characterized. During the course of the temperature stress tests, each time an oven was cooled for device testing, S-parameter measurements were made on about 20% of the FETs (same devices each measurement time). Table 2-7 gives typical initial measurements of S-parameters at 6 GHz for the low noise FET devices.

2.7 FAILURE CRITERIA

Two objectives of this investigation are to estimate the expected mean time to failure (MTTF) for operational GaAs FETs and to estimate the activation energy E_a of the primary failure mode. To do these required that we specify criteria for determining when a device has failed. The criteria adopted for this program are listed in Table 2-8, using the standard measurement conditions discussed in Sections 2.4 and 2.5. For two of the important DC parameters, I_{DSS} and g_m, functional failure of the GaAs FET is assumed to have occurred if one of these parameters has changed by 10% or more. The specific drain current I_{DS}, however, is allowed a larger variation (20%). The criteria are the same as those used by Hughes previously. These were based on the results of a sensitivity analysis of the equivalent circuit model for a Type N-2 low-noise GaAs FET.[3] Because most state-of-the-art FETs have similar equivalent circuits, in spite of differences in layout or processing, these failure criteria should also be reasonably valid for other types also. Section 5.8 discusses the effects of test design on the measured data.

TABLE 2-7

TYPICAL INITIAL MEASUREMENTS OF S-PARAMETERS AT 6 GHz FOR THE LOW NOISE FET DEVICES

Type Code	f, GHz	S_{11}		S_{21}		S_{12}		S_{22}	
		Mag	Phase	Mag	Phase	Mag	Phase	Mag	Phase
A-10	6	0.81	-79°	1.5	105°	0.05	37°	0.71	-38°
A-51	6	0.68	166	1.5	24	0.12	-21	0.36	-135
A-6	6	0.80	-92	2.2	103	0.07	38	0.65	-39
D-1	6	0.60	-156	1.3	27	0.04	-18	0.75	-95
D-22	6	0.75	-122	1.8	65	0.04	18	0.73	-66
D-2	6	0.83	-58	1.4	116	0.06	49	0.78	-30
H-1	6	0.72	-104	1.5	114	0.07	43	0.58	-53
H-11	6	0.72	-100	1.7	89	0.06	43	0.65	-49
H-1A1	6	0.60	-172	1.8	25	0.06	3.3	0.55	-103
H-21	6	0.90	-128	2.0	65	0.06	8	0.73	-65
N-21	6	0.78	-112	1.6	70	0.04	30	0.76	-53
N-3	6	0.80	-72	1.8	138	0.01	39	0.74	-39
N-31	6	0.81	-120	1.8	59	0.03	91	0.67	-87
N-32	6	0.81	-112	2.1	72	0.03	45	0.70	-70

Note: DC bias conditions were V_D = 3.5 V and I_D = 10 ma.

TABLE 2-8

LOW-NOISE GaAs FET ELECTRICAL FAILURE CRITERIA

Parameter	Prescribed Failure Limit
DC	
ΔI_{DS}	±20%
ΔI_{DSS}	±10%
Δg_m	±10%
RF	
ΔF_{min}	+0.5 dB
ΔG_a	-1.0 dB

Ultimately, of course, the microwave aging characteristics of the FETs become of greater operational importance than the DC characteristics. For low-noise amplifier applications we have assumed, as shown in Table 2-8, that an increase of 0.5 dB or more in minimum noise figure or a decrease of 1 dB or more in the associated gain represents reasonable limits for signifying RF operational failure. These failure criteria were taken from a previous program[2] and apply to measurements of device minimum noise figure in which the bias and input/output tuning conditions are adjusted each time to obtain F_{min}. An argument can be made for defining failure on the basis of measurements performed with specific fixed bias and tuning conditions, as these would represent the most likely conditions of circuit application. That approach was not taken on this program, however, because (1) considerable effort and expense would have been required to design, fabricate, and tune the necessary single-stage amplifiers; and (2) we are more interested in the aging characteristics of the FETs themselves than of circuits incorporating them. The techniques involved in measuring the RF parameters of a GaAs FET are generally more difficult, expensive, and time consuming than those required to measure its DC parameters. Also, RF measurement errors are significantly larger with respect to the failure criteria than are the DC measurements, as demonstrated on a previous program.[2] Therefore, throughout the accelerated life tests, we have relied on the DC failure criteria for determining device failure. The RF measurements were made on a more limited basis and were used to investigate the realtionships between DC and RF aging characteristics. Even though some investigators have concluded that there are no reliable or consistent relationships between DC parameter changes and RF failure, we believe that the DC data still provide valuable information with respect to device aging. Our data also show that there is some statistical correlation between DC and RF changes, although the considerable scatter tends to obscure this relationship for any single device.[2] Additional discussions on this topic are given in Sections 5.9 and 7.0.

During the tests, failure modes other than electrical failures were also observed and were usually obvious: open bond wire, cracked chip or substrate, loss of package hermeticity, etc. As our interest is in determining the MTTF at high temperatures and then extrapolating the results to lower normal operating temperatures, it is vital to select from the accumulated failure data those failure modes that were accelerated by the elevated temperature and, if possible, due to a single failure mechanism. Observed failure modes will be discussed in detail in subsequent sections.

3.0 PRELIMINARY DEVICE LOSSES

Significant numbers of FETs were initially inventoried, but were not able to be used in the formal testing program. Such devices are categorized as "preliminary device losses" and are discussed in this section. Table 3-1 categorizes the preliminary device losses and failures.

The categories of failure are somewhat arbitrary, as difficulties with the metallization or with wire bonding could feasibly be ascribed to inadequate operator training or skill. However, our technicians do competent work, and we have therefore chosen in general to categorize initial failures as due more to inadequate manufacturing than to inappropriate operator techniques.

Table 3-2 lists our resolution of the major difficulties with the low noise FET device types shown in Table 3-1. In the cases of FET types A-1 and H-1 we had purchased substantial numbers of devices, 50 and 76 units, respectively. When the suppliers were contacted about our difficulties with their devices, they immediately sent us replacement units of an improved type. In the cases of FET Types N-2, P-5, and R-5 we had purchased only about ten units each. As the testing of these devices had been planned not to be a major effort under this program, replacement devices were not sought from the suppliers.

Major preliminary device losses on similar devices procured for systems applications would have been prevented through a procedure of buying to necessary specifications and then implementing appropriate incoming inspections, including an initial burn-in period. As we wanted to receive devices for this program in the same condition as supplied by the manufacturer, we waived incoming inspection on all units. Consequently, we feel that no manufacturer's devices should be disqualified on the basis of our experience with these preliminary losses. It is our recommendation, therefore, that FET devices be purchased to satisfy needed specifications and be subjected to incoming inspection, and that the supplier be contacted immediately in the case of any problem. Without exception, we have found our vendors to be most cooperative.

TABLE 3-1

PRELIMINARY DEVICE LOSSES AND FAILURES

Type Code	Initial Inventory (Chip)	Loss Mode					
		Operator Learning	Physical Fracture	Contact Metal	Wire Bonds	Electrical (initial)	Total
A-1	50			50			50
A-6	50	5				10	15
A-10	15	1	1	3		1	6
D-1	11		1			2	3
D-2	11	2	1	2			5
H-1	76	20				1	21
H-11	15		1			1	2
N-2	10			9			9
N-3	61			3		2	5
P-4	3						0
P-5	11		1	4			5
R-2	2			1			1
R-5	11				10		10
Total	326	28	5	72	10	17	132

Note: In addition to the above chip losses, 21 packaged FETs were destroyed in preliminary testing, most of these failing during initial attempts to mount and apply bias to the FETs in the medium temperature ovens.

TABLE 3-2

RESOLUTION OF MAJOR PRELIMINARY DIFFICULTIES WITH LOW NOISE FET DEVICE TYPES

Type Code	Observation	Resolution
A-1	Gate bond pad gold metallization delaminated	Supplier replaced all FETs with improved units, Type A-6.
A-6	Source and drain were incorrectly identified on manufacturer's data sheet	Supplier furnished corrected data sheet.
H-1	Dice were brittle; gold-aluminum alloy formed	Supplier provided improved units, Type H-11.
N-2	Bond pad gold metallization delaminated	These widely used FETs may have had a lot or operator problem. A higher reliability grade FET should be specified.
P-5	Bond pads had thin gold metallization over hard metal, causing bonding difficulties	Bonding wires were smeared in to make contact.
R-5	Bonding pads were badly scarred from previous testing	Avoid excessive testing.

Note: Incoming inspection was waived on all units.

4.0 ENVIRONMENTAL CHARACTERIZATION

Environmental characterization refers to tests conducted for the purpose of determining device reliability under various environmental conditions. We chose to characterize the packaged FETs, rather than the FET chips, because chip devices are normally used in hermetically sealed enclosures where humidity is low. The FET metallizations are known to be thin, and the susceptibility of the metals to degradation in various humidity and corrosive environments is well known from silicon device technology. Therefore, we felt it more important to characterize the packaged FETs, because one has the impression that they should be rather immune to environmental effects.

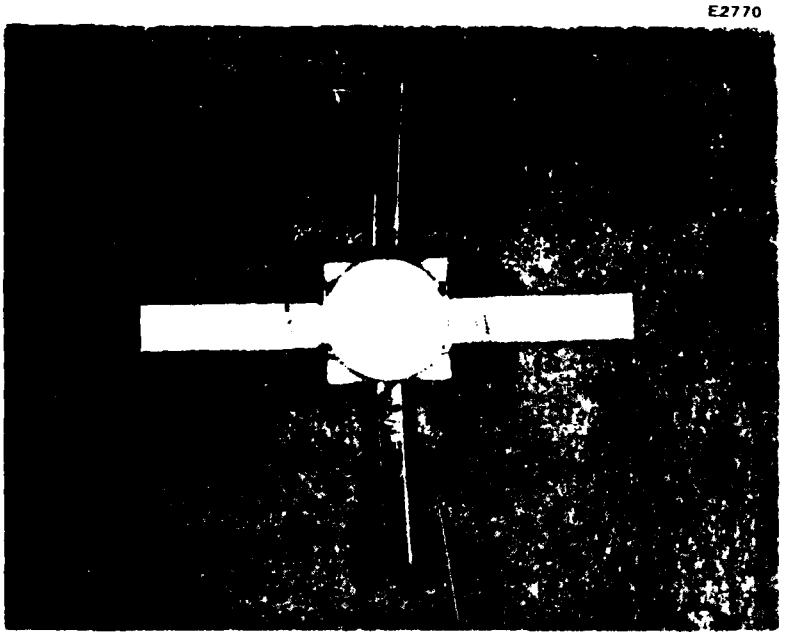
4.1 PACKAGE STYLES

A presentation of package styles was reserved for this section because the question of package reliability first arises in a discussion of environmental tests. Packaged devices were used also in the low temperature tests discussed later.

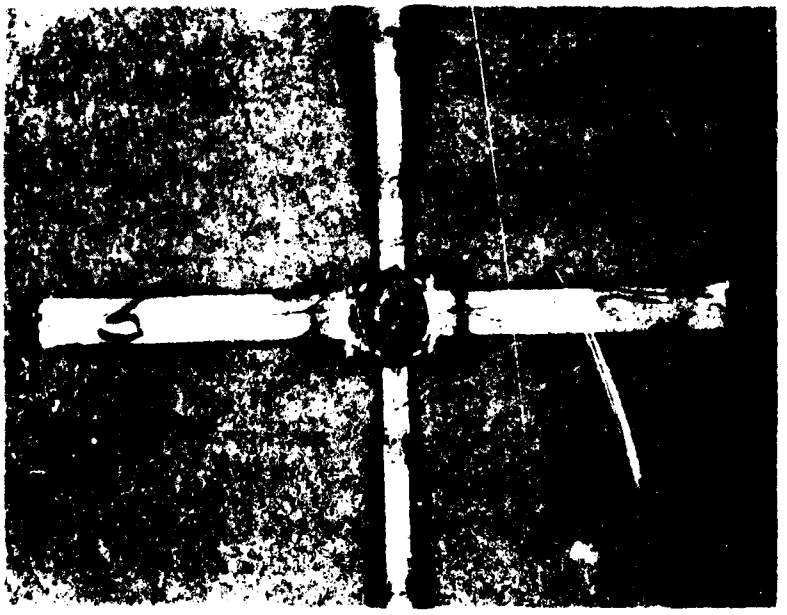
Photographs of package styles for FETs used in environmental tests are shown in Figures 4-1 through 4-4. These include 70 mil and 100 mil microstrip packages, as well as the large H-21 package, the large 140 mil N-31 package, and the P-51 stud package. Both R-51 FETs were the only packaged devices showing hermeticity failure. These two FETs were also the only packaged devices that exhibited internal failures during the course of the environmental testing sequence.

4.2 ENVIRONMENTAL TESTS

Environmental tests performed on the low noise packaged FETs were temperature cycling, acceleration, random vibration, and mechanical shock. Hermeticity was checked at every step. We did not do salt-spray and humidity tests, preferring instead to measure possible package leaks directly. We were primarily interested in issues such as wire and die bond integrity and damage to the small packages during these tests.



(a)



(b)

Figure 4-1 (a) Type R-51. (b) Type D-1.

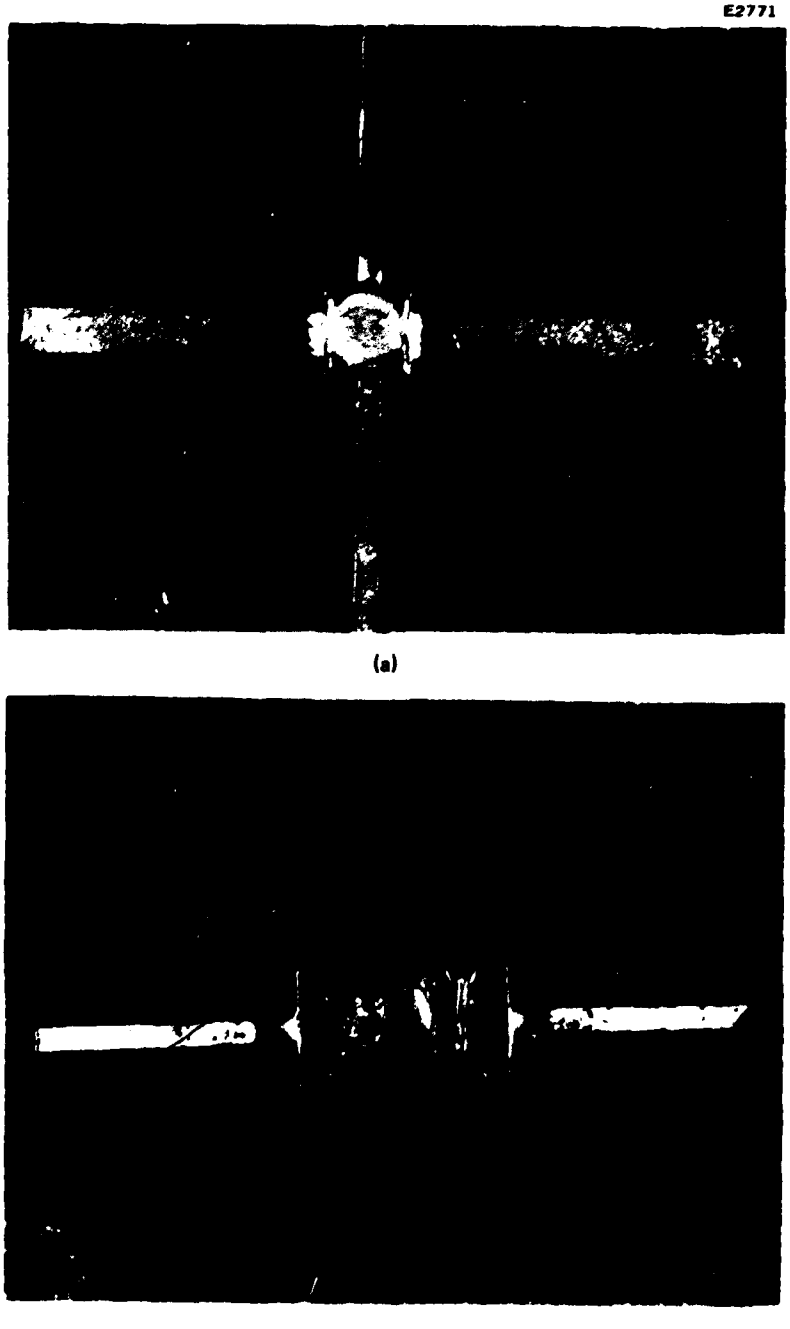
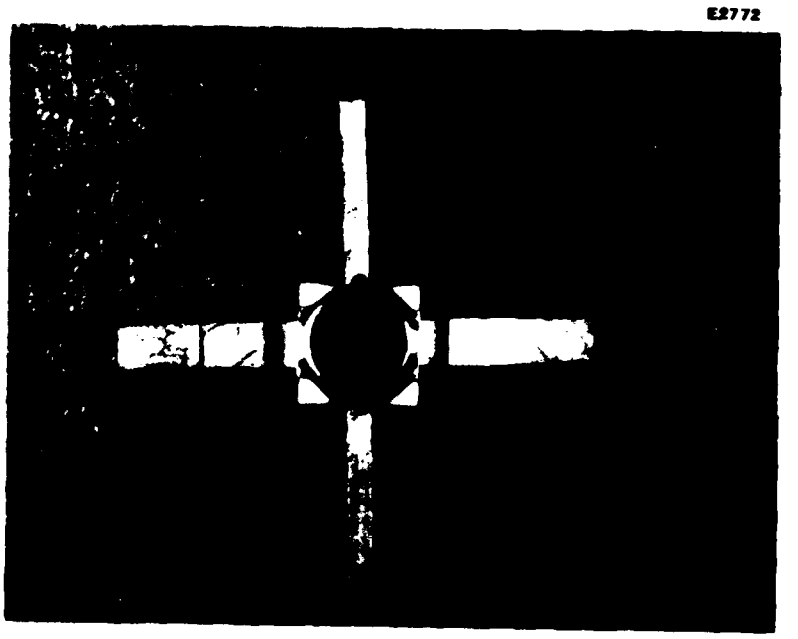
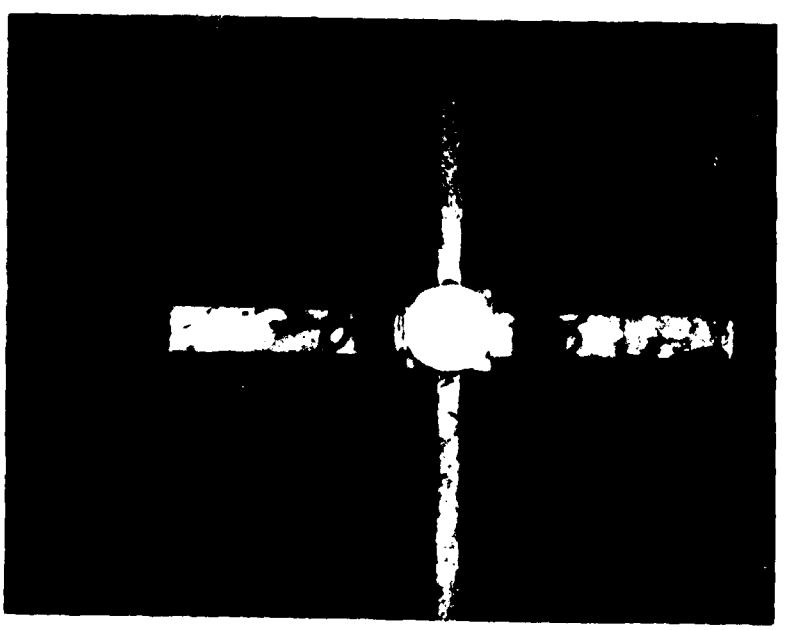


Figure 4-2 (a) Type D-2. (b) Type H-21.



(a)



(b)

Figure 4-3 (a) Type H-1A1. (b) Type N-21.

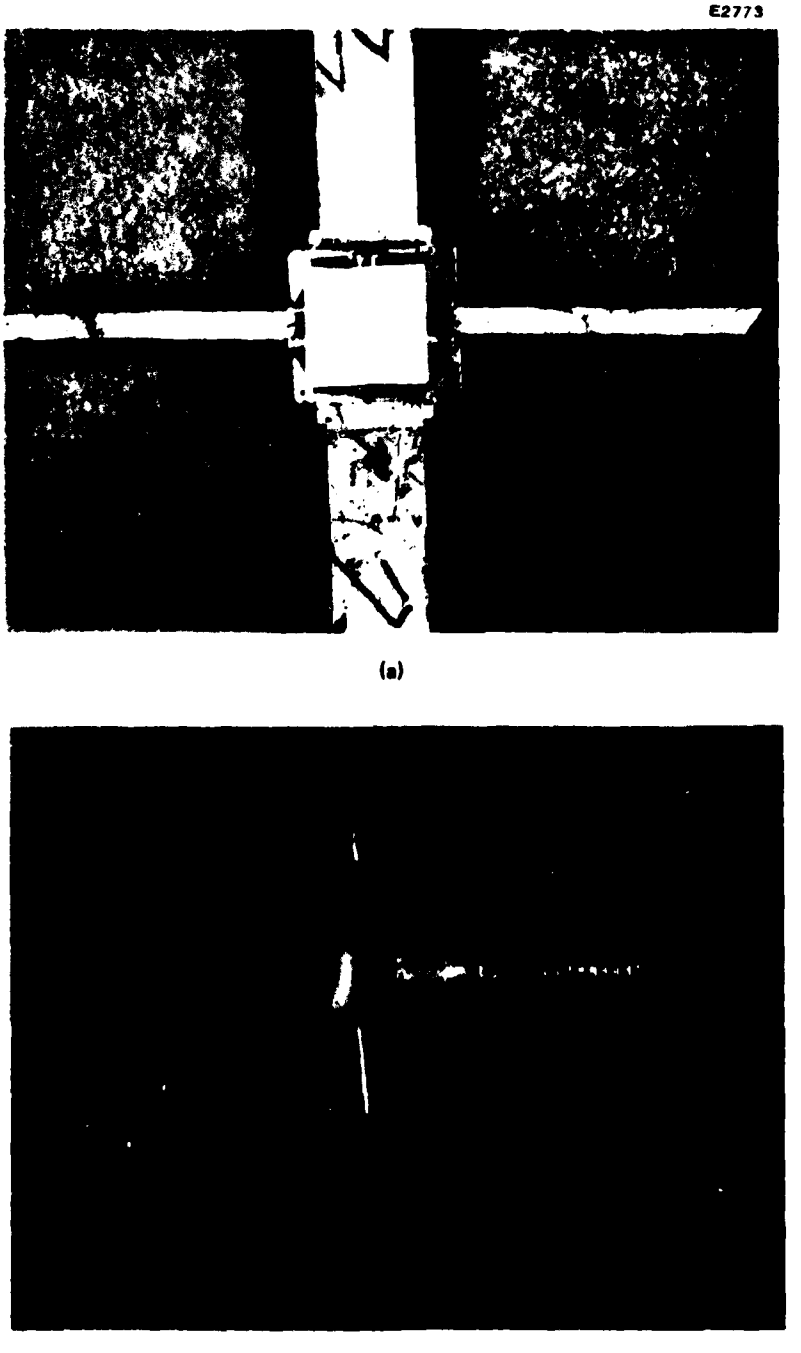


Figure 4-4 (a) Type N-31. (b) Type P-51.

These packaged devices were handled using accepted static suppression techniques. E-Kote 3030 (silver paint) was applied as a terminal shorting system before the devices were transferred from the electrical test site to the environmental test site. The paint was removed with solvent prior to all DC test steps. The porosity of the paint was considered to be a potential source of misleading helium leak test information, but no problem appeared.

Complete environmental test data on the 16 devices are given in Tables 4-1 through 4-8. All tests conformed to the applicable MIL-standard, as listed in the left column of these tables. In addition, two type D-22 FETs were included in the test group as controls to give confidence in the other device measurements. They were given the same DC tests as the test devices at each stage, but they underwent no environmental testing. Measurements on these two type D-22 control devices are shown in Table 4-9. The consistency of the measurements validates the data from the test devices.

4.3 FAILURE ANALYSIS OF ENVIRONMENTAL FAILURES

Failures of devices assigned to the environmental testing procedures were observed as follows:

1. A Type P-51 device apparently failed temperature cycling when a 3300-fold increase in the reverse gate current was observed.

2. A Type R-51 device failed the hermeticity test after random vibration. (Device No. 11).

3. A Type R-51 device failed the initial hermeticity test. This device was kept in the environmental test sequence and later failed after random vibration due to a drain-source short. (Device No. 1.)

Because the third device listed above had already failed hermeticity before the formal environmental testing sequence had begun, strictly speaking, failure of this device cannot be accounted to the environmental testing program. However, as the later drain-source short, which appears unrelated to the non-hermeticity of the package,

TABLE 4-1

MEASUREMENTS ON D-11 DEVICES FOR ENVIRONMENTAL CHARACTERIZATION TESTS

DEVICE D-11 NO. OF DEVICES 2

Test Sequence and the Test Specification Used	Device No.	I_{DS}, mA V_D = 0.5V	V_p, V I_D = 100 µA V_D = 3.0V	I_G, µA	Hermeticity, Std. cc/sec. He
1.0 Initial DC test and Hermeticity per MIL-S-883B, Sect. 1014.2(A)	4	24	-1.60	-3.0 @ -17V	3.5×10^{-9}
	5	22	-1.75	-3.0 @ -19V	4.0×10^{-9}
2.0 Temp Cycle: MIL-S-883B, Sect. 1010.2(C), Step 2,4					
3.0 DC Test and Hermeticity as at (1.0)	4	24	-1.60	-3.0	5.0×10^{-9}
	5	21	-1.75	-3.0	5.0×10^{-9}
4.0 Acceleration: MIL-S-883B, Sect. 2001.2(c), Y1, 20 Kg's					
5.0 DC Test and Hermeticity as at (1.0)	4	23	-1.58	-3.0	5.0×10^{-9}
	5	20	-1.74	-3.0	5.0×10^{-9}
6.0 Random Vibration: MIL-S-202 15g, 45g, 60g, Y1 Axis					
7.0 DC Test and Hermeticity as at (1.0)	4	22	-1.60	-3.0	5.0×10^{-9}
	5	21	-1.76	-3.0	5.5×10^{-9}
8.0 Mech Shock: MIL-S-883B Sect. 2002.2(C) Y1, 3 Kg's					
9.0 DC Test and Hermeticity as at (1.0)	4	19	-1.61	-3.0	5.5×10^{-9}
	5	18	-1.78	-3.0	5.5×10^{-9}

TABLE 4-2

MEASUREMENTS ON D-22 DEVICES FOR ENVIRONMENTAL CHARACTERIZATION TESTS

DEVICE D-22				NO. OF DEVICES 2	
Test Sequence and the Test Specification Used	Device No.	I_{DS}, mA V_D = 0.5V	V_p, V I_D = 100 µA V_D = 3.0V	I_G, µA	Hermeticity, Std. cc/sec. He
1.0 Initial DC test and Hermeticity per MIL-S-883B, Sect. 1014.2(A)	9	17	-1.87	-3.0 @ -8V	5×10^{-9}
	10	17	-1.65	-3.0 @ -8V	5×10^{-9}
2.0 Temp Cycle: MIL-S-883B, Sect. 1010.2(C), Step 2, 4					
3.0 DC Test and Hermeticity as at (1.0)	9	17	-1.86	-3.0	5×10^{-9}
	10	17	-1.65	-3.0	5×10^{-9}
4.0 Acceleration: MIL-S-883B, Sect. 2001.2(C), Y1, 20 Kg's					
5.0 DC Test and Hermeticity as at (1.0)	9	16	-1.84	-3.0	5×10^{-9}
	10	17	-1.65	-3.0	5×10^{-9}
6.0 Random Vibration: MIL-S-202 15g, 45g, 60g, Y1 Axis					
7.0 DC Test and Hermeticity as at (1.0)	9	17	-1.84	-3.0	5×10^{-9}
	10	17	-1.65	-3.0	5×10^{-9}
8.0 Mech Shock: MIL-S-883B Sect. 2002.2(C) Y1, 3 Kg's					
9.0 DC Test and Hermeticity as at (1.0)	9	17	-1.80	-3.0	5×10^{-9}
	10	17	-1.63	-3.0	5×10^{-9}

TABLE 4-3

MEASUREMENTS ON H-1A1 DEVICES FOR ENVIRONMENTAL CHARACTERIZATION TESTS

DEVICE H-1A1 NO. OF DEVICES 2

Test Sequence and the Test Specification Used	Device No.	I_{DS}, mA V_D = 0.5V	V_p, V I_D = 100 µA V_D = 3.0V	I_G, µA	Hermeticity, Std. cc/sec. He
1.0 Initial DC test and Hermeticity per MIL-S-883B, Sect. 1014.2(A)	1	40	-3.50	-3.0 @ -6V	3.5×10^{-9}
	11	38	-2.75	-3.0 @ -9V	3.0×10^{-9}
2.0 Temp Cycle: MIL-S-883B, Sect. 1010.2(C), Step 2,4					
3.0 DC Test and Hermeticity as at (1.0)	1	40	-2.90	-3.0	4.0×10^{-9}
	11	36	-2.64	-3.0	4.0×10^{-9}
4.0 Acceleration: MIL-S-883B, Sect. 2001.2(C), Y1, 20 Kg's					
5.0 DC Test and Hermeticity as at (1.0)	1	40	-2.83	-3.0	4.0×10^{-9}
	11	36	-2.64	-3.0	4.5×10^{-9}
6.0 Random Vibration: MIL-S-202 15g, 45g, 60g, Y1 Axis					
7.0 DC Test and Hermeticity as at (1.0)	1	37	-2.87	-3.0	5.0×10^{-9}
	11	34	-2.66	-3.0	5×10^{-9}
8.0 Mech Shock: MIL-S-883B Sect. 2002.2(C) Y1, 3 Kg's					
9.0 DC Test and Hermeticity as at (1.0)	1	35	-2.85	-3.0	5.0×10^{-9}
	11	34	-2.67	-3.0	6.0×10^{-9}

TABLE 4-4

MEASUREMENTS ON H-21 DEVICES FOR ENVIRONMENTAL CHARACTERIZATION TESTS

DEVICE H-21 NO. OF DEVICES 2

Test Sequence and the Test Specification Used	Device No.	I_{DS}, mA V_D = 0.5V	V_p, V I_D = 100 µA V_D = 3.0V	I_G, µA	Hermeticity, Std. cc/sec. He
1.0 Initial DC test and Hermeticity per MIL-S-883B, Sect. 1014.2(A)	1	26	-2.20	-3.0 @ -5V	3.0×10^{-9}
	11	23	-1.54	-3.0 @ -5V	3.5×10^{-9}
2.0 Temp Cycle: MIL-S-883B, Sect. 1010.2(C), Step 2,4					
3.0 DC Test and Hermeticity as at (1.0)	1	30	-2.20	-3.0	5.0×10^{-9}
	11	23	-1.54	-3.0	5.0×10^{-9}
4.0 Acceleration: MIL-S-883B, Sect. 2001.2(C), Y1, 20 Kg's					
5.0 DC Test and Hermeticity as at (1.0)	1	21	-2.20	-3.0	4.0×10^{-9}
	11	17*	-1.53	-3.0	6.0×10^{-9}
6.0 Random Vibration: MIL-S-202 15g, 45g 60g, Y1 Axis					
7.0 DC Test and Hermeticity as at (1.0)	1	20*	-2.10	-3.0	5.0×10^{-9}
	11	17	-1.53	-3.0	5.0×10^{-9}
8.0 Mech Shock: MIL-S-883B Sect. 2002.2(C) Y1, 3 Kg's					
9.0 DC Test and Hermeticity as at (1.0)	1	30	-2.23	-3.0	5.0×10^{-9}
	11	17	-1.54	-3.0	5.0×10^{-9}

*Not a drain current failure - see text.

TABLE 4-5

MEASUREMENTS ON N-21 DEVICES FOR ENVIRONMENTAL CHARACTERIZATION TESTS

DEVICE N-21 NO. OF DEVICES 2

Test Sequence and the Test Specification Used	Device No.	I_{DS}, mA V_D = 0.5V	V_p, V I_D = 100 µA V_D = 3.0V	I_G, µA	Hermeticity, Std. cc/sec. He
1.0 Initial DC test and Hermeticity per MIL-S-883B, Sect. 1014.2(A)	1	44	-4.00	-3.0 @ -13V	4.0×10^{-9}
	37	25	-2.20	-3.0 @ -23V	4.0×10^{-9}
2.0 Temp Cycle: MIL-S-883B, Sect. 1010.2(C), Step 2,4					
3.0 DC Test and Hermeticity as at (1.0)	1	44	-3.94	-3.0	5.0×10^{-9}
	37	23	-2.19	-3.0	7.5×10^{-9}
4.0 Acceleration: MIL-S-883B, Sect. 2001.2(C), Y1, 20 Kg's					
5.0 DC Test and Hermeticity as at (1.0)	1	41	-3.94	-3.0	5.0×10^{-9}
	37	23	-2.17	-3.0	6.0×10^{-9}
6.0 Random Vibration: MIL-S-202 15g, 45g, 60g, Y1 Axis					
7.0 DC Test and Hermeticity as at (1.0)	1	41	-3.94	-3.0	5.5×10^{-9}
	37	23	-2.17	-3.0	5.0×10^{-9}
8.0 Mech Shock: MIL-S-883B Sect. 2002.2(C) Y1, 3 Kg's					
9.0 DC Test and Hermeticity as at (1.0)	1	40	-3.94	-3.0 @ -10V	5.0×10^{-9}
	37	23	-2.19	-3.0	5.0×10^{-9}

TABLE 4-6

MEASUREMENTS ON N-31 DEVICES FOR ENVIRONMENTAL CHARACTERIZATION TESTS

DEVICE N-31 NO. OF DEVICES 2

Test Sequence and the Test Specification Used	Device No.	I_{DS}, mA V_D = 0.5V	V_p, V I_D = 100 µA V_D = 3.0V	I_G, µA	Hermeticity, Std. cc/sec. He
1.0 Initial DC test and Hermeticity per MIL-S-883B, Sect. 1014.2(A)	45	32	-1.65	-3.0 @ -12V	4.0×10^{-9}
	50	48	-3.00	-3.0 @ -10V	3.5×10^{-9}
2.0 Temp Cycle: MIL-S-883B, Sect. 1010.2(C), Step 2,4					
3.0 DC Test and Hermeticity as at (1.0)	45	31	-1.64	-3.0	8.0×10^{-9}
	50	49	-2.97	-3.0	5.0×10^{-9}
4.0 Acceleration: MIL-S-883B, Sect. 2001.2(C), Y1, 20 Kg's					
5.0 DC Test and Hermeticity as at (1.0)	45	30	-1.64	-3.0	4.5×10^{-9}
	50	48	-2.85	-3.0	4.0×10^{-9}
6.0 Random Vibration: MIL-S-202 15g, 45g, 60g, Y1 Axis					
7.0 DC Test and Hermeticity as at (1.0)	45	30	-1.64	-3.0	5.0×10^{-9}
	50	43	-2.80	-3.0	5.0×10^{-9}
8.0 Mech Shock: MIL-S-883B Sect. 2002.2(C) Y1, 3 Kg's					
9.0 DC Test and Hermeticity as at (1.0)	45	30	-1.64	-3.0	6.5×10^{-9}
	50	43	-2.85	-3.0	5.0×10^{-9}

TABLE 4-7

MEASUREMENTS ON P-51 DEVICES FOR ENVIRONMENTAL CHARACTERIZATION TESTS

DEVICE P-51				NO. OF DEVICES 2	
Test Sequence and the Test Specification Used	Device No.	I_{DS}, mA V_D = 0.5V	V_p, V I_D = 100 µA V_D = 3.0V	I_G, µA	Hermeticity, Std. cc/sec. He
1.0 Initial DC test and Hermeticity per MIL-S-883B, Sect. 1014.2(A)	1	20*	-2.75	-3.0 @ -11V	3.0×10^{-9}
	11	40	-3.20	-3.0 @ -9V	4.0×10^{-9}
2.0 Temp Cycle: MIL-S-883B, Sect. 1010.2(C), Step 2,4					
3.0 DC Test and Hermeticity as at (1.0)	1	30*	-2.67	-3.0	5.5×10^{-9}
	11	42	-3.10	Withdrawn for failure analysis when I_G went to -10 mA @ -0.5V (not a gate current failure - see text)	
4.0 Acceleration: MIL-S-883B, Sect. 2001.2(C), Y1, 20 Kg's					
5.0 DC Test and Hermeticity as at (1.0)	1	33	-2.65	-3.0	6.5×10^{-9}
	11	--	--	--	--
6.0 Random Vibration: MIL-S-202 15g, 45g, 60g, Y1 Axis					
7.0 DC Test and Hermeticity as at (1.0)	1	30	-2.64	-3.0	5.5×10^{-9}
	11	--	--	--	--
8.0 Mech Shock: MIL-S-883B Sect. 2002.2(C) Y1, 3 Kg's					
9.0 DC Test and Hermeticity as at (1.0)	1	31	-2.60	-3.0	5.5×10^{-9}
	11	--	--	--	--

*Not a drain current failure - see text.

TABLE 4-8

MEASUREMENTS ON R-51 DEVICES FOR ENVIRONMENTAL CHARACTERIZATION TESTS

DEVICE R-51 NO. OF DEVICES 2

Test Sequence and the Test Specification Used	Device No.	I_{DS}, mA V_D = 0.5V	V_p, V I_D = 100 µA V_D = 3.0V	I_G, µA	Hermeticity, Std. cc/sec. He
1.0 Initial DC test and Hermeticity per MIL-S-883B, Sect. 1014.2(A)	1	17	-1.05	-3.0 @ -7V	5.0×10^{-7}*
	11	19	-1.35	-3.0 @ -10V	4.5×10^{-9}
2.0 Temp Cycle: MIL-S-883B, Sect. 1010.2(C), Step 2,4					
3.0 DC Te · and Hermeticity as at (1.0)	1	17	-1.07	-3.0	4.3×10^{-7}
	11	17	-1.32	-3.0	4.0×10^{-9}
4.0 Acceleration: MIL-S-883B, Sect. 2001.2(C), Y1, 20 Kg's					
5.0 DC Test and Hermeticity as at (1.0)	1	17	-1.07	-3.0 @ -5.5V	1.5×10^{-7}
	11	17	-1.31	-3.0	4.5×10^{-9}
6.0 Random Vibration: MIL-S-202 15g, 45g, 60g, Y1 Axis					
7.0 DC Test and Hermeticity as at (1.0)	1	Removed for failure analysis - drain/source short			
	11	16	-1.31	-3.0	7.0×10^{-7}*
8.0 Mech Shock: MIL-S-883B Sect. 2002.2(C) Y1, 3 Kg's					
9.0 DC Test and Hermeticity as at (1.0)	1	--	--	--	--
	11	15	-1.27	-3.0	1.0×10^{-8}

*Hermeticity failure - allowed to remain in sequence.

TABLE 4-9

MEASUREMENTS ON D-22 CONTROL DEVICES FOR ENVIRONMENTAL CHARACTERIZATION TESTS

DEVICE D-22				NO. OF DEVICES 2	
Test Sequence and the Test Specification Used	Device No.	I_{DS}, mA V_D = 0.5V	V_p, V I_D = 100 µA V_D = 3.0V	I_G, µA	Hermeticity, Std. cc/sec. He
1.0 Initial DC test and Hermeticity per MIL-S-883B, Sect. 1014.2(A)	11	19	-1.95	-3.0 @ -6V	Not Done - Control Devices
	2	30	-2.27	-3.0 @ -14V	
2.0 Temp Cycle: MIL-S-883B, Sect. 1010.2(C), Step 2.4	Not Done - Control Devices				
3.0 DC Test and Hermeticity as at (1.0)	11	19	-1.93	-3.0	--
	2	29	-2.26	-3.0	--
4.0 Acceleration: MIL-S-883B, Sect. 2001.2(C), Y1, 20 Kg's	Not Done - Control Devices				
5.0 DC Test and Hermeticity as at (1.0)	11	18	-1.92	-3.0	--
	2	28	-2.28	-3.0	--
6.0 Random Vibration: MIL-S-202 15g, 46g, 60g, Y1 Axis	Not Done - Control Devices				
7.0 DC Test and Hermeticity as at (1.0)	11	18	-1.89	-3.0	--
	2	30	-2.27	-3.0	--
8.0 Mech Shock: MIL-S-883B Sect. 2002.2(C) Y1, 3 Kg's	Not Done - Control Devices				
9.0 DC Test and Hermeticity as at (1.0)	11	16	-1.92	-3.0	--
	2	30	-2.29	-3.0	--

occurred during the environmental testing sequence, failure analysis of this device is included here in the environmental section rather than in the previous section on Preliminary Device Losses.

The apparent failure of the Type P-51 device was discovered to be due to a sliver of the E-Kote 3030 shorting paint across the gate lead. When the paint was completely removed, the device tested good.

Close visual inspection of the two Type R-51 devices that failed the hermeticity test disclosed no apparent irregularities in fabrication. However, we delidded Device No. 11 anyway for internal inspection, as part of our standard failure analysis procedures. We then discovered alloying of the gold-tin eutectic die bonding material with the source bond wires. Figure 4-5 shows a SEM photograph of the failed FET. Necking down of a source bond wire is particularly apparent near the bottom of the photograph.

Judging from the character of the alloying, we doubt that the alloying could have occurred during wire bonding. Wire bonding temperatures were usually not high enough to result in that much alloying. This is a subjective judgment, however, and is conditioned by the belief that the vendor would have rejected such a part in the pre-cap visual inspection. A more likely cause of the alloying is overheating during sealing of the cap, which was also done using gold-tin. The obvious solution to this problem is to limit the amount of eutetic material used during die bonding. Also, the source wires should not be bonded to the area wetted by the eutectic. This sort of incipient failure indicates that high reliability parts should be delidded as part of the qualification process to assure that the die bond is properly formed and that proper source bond lead dress is achieved.

The final low noise FET from the environmental characterization tests to undergo failure analysis was opened and examined. It was a Type R-51, our Device Number 1. We found that the FET die had cracked approximately in half. One portion was still attached to the header, and one piece was held in the package by the drain wire. In the failure the drain wire apparently short circuited to a source wire or ground.

E2746

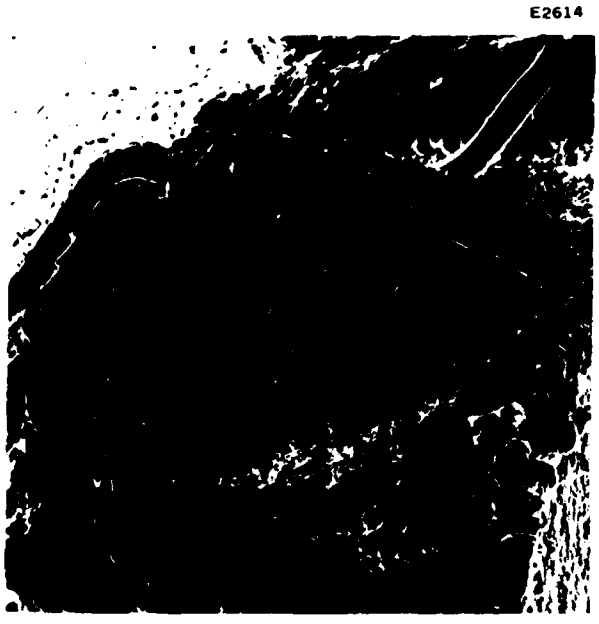
Figure 4-5 Type R-51, showing failure of source bond wires.

Figure 4-6 is a SEM photograph of the piece of die whch remained attached to the header. Prolonged examination of the package in the SEM and under the optical microscope failed to reveal any evidence of GaAs on the header surface from which the piece of die had become detached. We concluded that the die had fractured during the random vibration test, which consisted of successive states at 15g, 45g and 60g along one axis. In this case the axis was perpendicular to the die mounting surface.

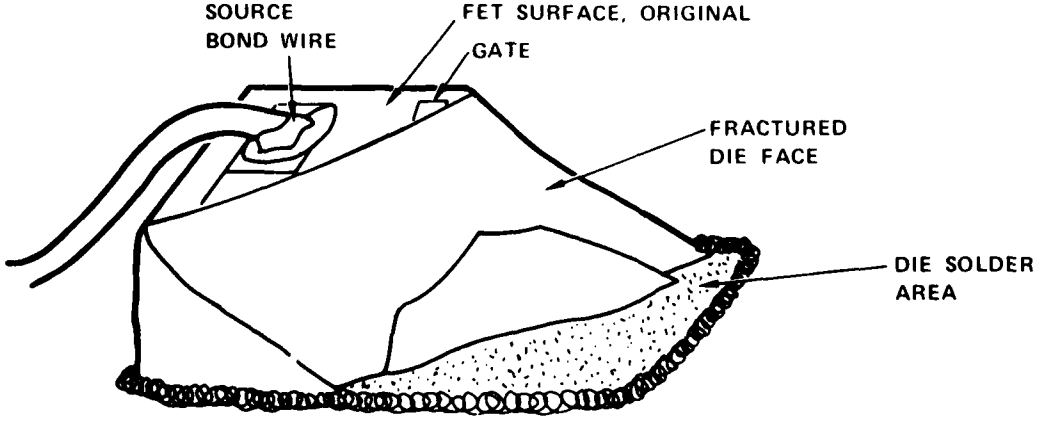
We hypothesize that the die was not completely wetted to the header solder and likely was cantilevered on one edge, the edge which is still attached. The test vibration probably caused the fracture. For the population of all devices tested, this represents 1 failure in 15. The failure is probably due to a quality control problem in die attach rather than indicating anything fundamental with regard to the GaAs FET. On the other hand, one might observe that, because of the more brittle nature of GaAs, the FETs may be less tolerant of insecure die mounting than silicon dice would be.

As a result of these tests we would recommend that packaged FETs be subjected to 100% vibration screening tests for any critical application, such as military or satellite use. Power FETs should be especially vulnerable to vibration failures, because of the large die areas.

Three instances occurred where the reported drain current apparently exceeded the change limits allowed in Table 2-8. The devices were Type H-21, #1 and #11, and Type P-51, #1. In the environmental testing sequence we were mainly concerned with failures that might be directly connected with the environmental tests. Our operators were instructed to determine whether there were any major changes in the electrical parameters, indicating gross problems. Measuring the drain current required pressure contacting of the drain and source leads. Variations in the contact resistance would, of course, result in different readings for the drain current. We suspect that the anomalous drain current readings for the three devices mentioned were of this nature and not actual ΔI_{DS} failures. In later tests on packaged devices we took additional steps to assure accurate drain current measurements.



(a)



(b)

Figure 4-6 Type R-51, #1, which failed during the random vibration test. (a) SEM photograph of fractured die, 600X. (b) Sketch identifying areas of interest.

5.0 HIGH TEMPERATURE CONSTANT STRESS TESTS ON FET CHIPS

Constant stress tests on electronic components at elevated temperatures have been the classical method for estimating the mean time to failure at normal operating temperatures and also the activation energy. The aging characteristics and operational life times of the low noise FET chips have been investigated by subjecting test samples to accelerated life tests at elevated ambient temperatures, under both unbiased and low-noise-biased conditions. Visual, DC, and RF characteristics and S-parameters of the devices were monitored periodically during these tests, and the DC results were used to determine the mean time-to-failure and activation energy. Correlation of RF and DC results is discussed, and primary failure observations are described.

5.1 TEST APPROACH

The accelerated life tests were of the constant-stress type. This statement means that the samples were subjected to constant temperature and electrical stress levels throughout the test period. The only changes in stress levels occurred when the bias was removed and the samples were brought to room temperature for the periodic characterization measurements. After being characterized, the samples were returned to their designated elevated stress levels and the next cycle was started.

The constant-stress life tests were performed in bias ovens of a type originally developed by the Hughes Research Laboratories (HRL) for life testing semiconductor devices. Figure 5-1 shows one of these ovens with its insulated cover removed. The heart of the oven consists of a stainless steel block that is heated along its full length by a cartridge heater. The GaAs FET chip test samples on their alumina microstrip carriers were mounted in the chamber of the stainless steel block and covered by a quartz lid. During operation, to keep the chips clean and dry the oven chamber was continually purged with slowly flowing dry nitrogen derived from a liquid source.

Each oven has 10 positions for DC-biased samples and approximately 20 positions for unbiased samples. The alumina microstrip carriers of the biased devices were firmly held in place with clamps, as shown in Figure 5-1. The unbiased devices were simply placed on top of the clamps. Gate and drain bias lines were brought into each sample

E2774

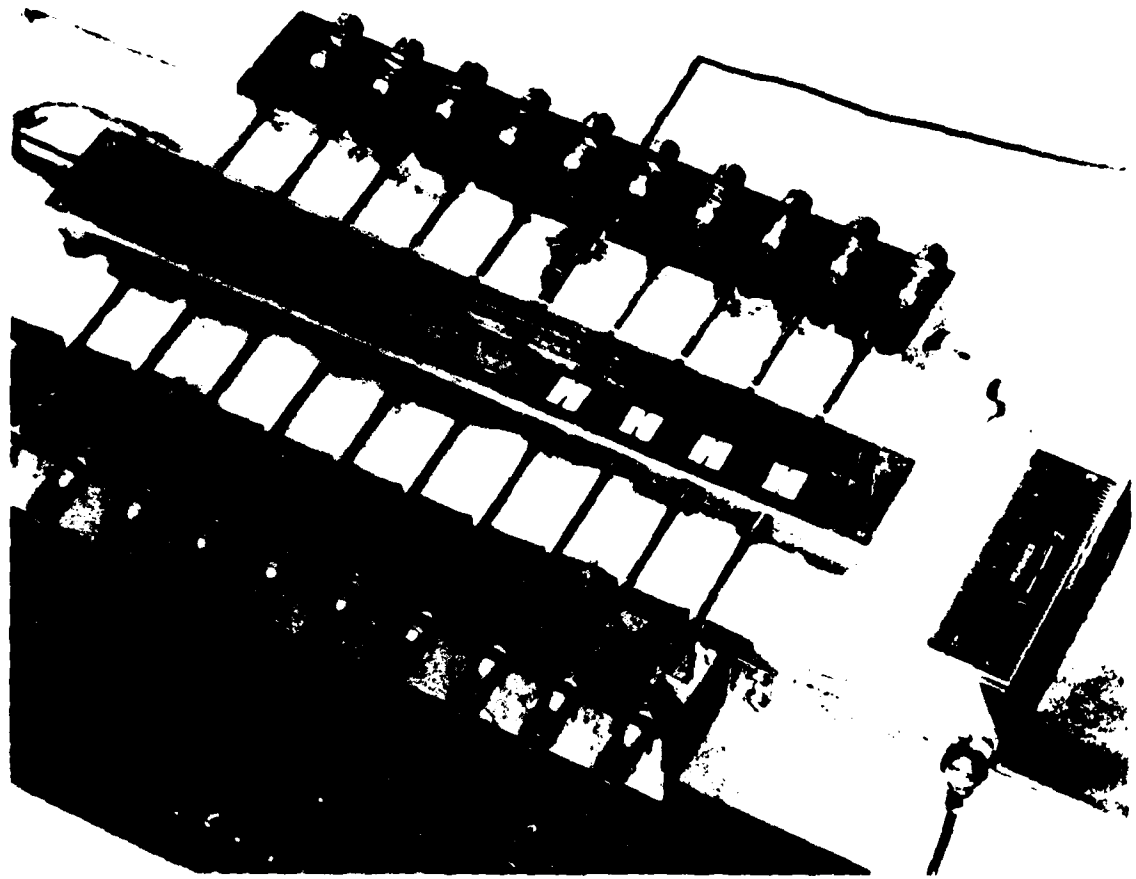


Figure 5-1 HRL-developed bias oven with the insulated cover removed. The samples in positions 1 through 6 are covered by the hold-down clamps; those in positions 7 through 10 are shown uncovered. During operation the alumina microstrip carriers of all biased FETs are held down with the clamps.

position with 50-ohm coaxial transmission lines consisting of coaxial stainless steel and glass tubing and nickel wire. These coaxial lines extended through the insulated walls of the oven to the outside where, at room temperature, the coaxial lines connected to gate and drain bias filters. These were essentially low-pass RC filters that acted to reduce any tendency of the biased FETs to oscillate. A schematic of the bias circuit for an oven is shown in Figure 5-2. All the biased FETs in an oven shared common gate and drain DC power supplies. Individual voltage dividers were inserted between the gate supply bus and the individual gate bias filters. These allowed separate gate bias control of each test sample.

The low noise bias conditions used throughout these tests are V_{DB} = 5 V and I_D = 10 mA. The voltage on the drain after voltage drop through the load resistor is V_D = 4 V. Hughes previously used V_D = 5 V because it was close to optimal for low-noise GaAs FET amplifiers when noise figure, gain, and third-order intermodulation are considered. However, most data sheets cite V_D = 3 V to 4 V. We believe that 4 V represents a more realistic electrical stress level for simulating actual operational bias stress than 5 V with the present FETs.

Thermal resistance of the individual devices was not measured; however, nominal values are given in Table 2-2 for some devices. Consequently, although we know the DC power input, the temperature of the channel cannot be determined accurately. The biased low noise devices, therefore, will have somewhat higher channel temperatures than unbiased devices.

In addition to the higher channel temperature of the biased devices, other test conditions were also different for biased FETs, compared to unbiased units. The different mounting procedures and the amount of handling need to be taken into account when interpreting the results. This topic is further considered in Section 5.3. Our general conclusions will still be valid, provided we are appropriately cautious with comparisons between biased and unbiased results.

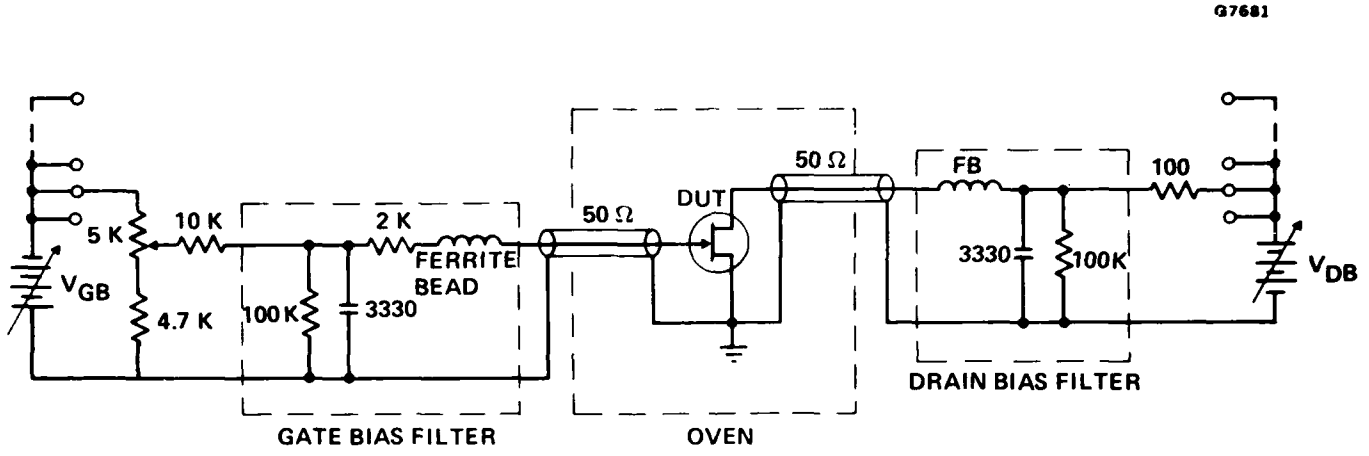


Figure 5-2 Schematic of the bias circuits for a test oven.

5.2 SUMMARY OF HIGH TEMPERATURE TESTS

Each FET chip assigned to the high temperature constant stress tests was assigned a serial number. The Appendix has detailed information on the status of each serialized FET. On devices that did not fail the cumulative number of operating hours is given. For failed devices the observation that confirmed the failure is noted, along with the cumulative operating hours to failure. In Table A-1 "Run No." refers to a specific oven loading. Some devices were biased and some were unbiased, as indicated by "B" and "U", respectively.

A summary of the high temperature constant stress tests on FET chip devices compiled from information in Table A-1 is shown in Table 5-1. "B" and "U" refer to biased and unbiased devices, respectively. Seven ovens of the type shown in Figure 5-1 were used with a stress temperature of 200°C, 220°C, 240°C, or 260°C. At the higher temperatures the total test times were sufficiently short that we were able to perform more than one temperature stress test in an oven during the course of the program.

After the oven tests were started, the ovens were periodically brought back to room temperature. The FETs were retested for DC parameters on a 100% basis and for RF and S-parameter data on a sampling basis, as explained in Sections 2.4 and 2.5. A time schedule was established for testing the devices throughout the course of the high temperature constant stress program. The testing schedule was planned with our best estimates of when the FETs should be tested. Devices being stressed at the higher temperatures were, of course, to be tested more frequently. Early in the program, however, the testing sequence was found to be so long that in some runs all devices had failed by the time of the first cooling of the ovens. One reason for this situation was lack of a suitable burn-in period, as explained in Section 5.3. Another reason was that a manufacturer may still have been perfecting his processing, as was the case with the A-6 devices.[1]

TABLE 5-1

SUMMARY OF HIGH TEMPERATURE CONSTANT STRESS
TESTS ON FET CHIP DEVICES

Type Code	Oven No.	Temp °C	Run No.	No. FETs Started		Begin Date	End Date	No. FETs Failed	
				B	U			B	U
H-1	1	200	2	9	4	7/17/79	1/23/80	9	4
A-6	1	260	9	4	3	1/29/80	2/20/80	4	3
A-10	1	260	10	5	3	3/13/80	6/19/80	4	2
N-3	2	200	1	10	4	8/24/79	7/14/80	10	4
H-1	3	220	3	10	4	9/27/79	6/23/80	10	4
N-3	4	220	4	11	4	9/28/79	1/15/80	10	4
D-1	5	240	6	5	2	11/15/79	7/16/80	5	2
D-2	5	240	6	5	0	11/15/79	7/16/80	4	0
P-5	6	240	5	4	1	11/13/79	11/27/79	4	1
A-6	6	240	8	9	4	12/14/79	2/07/80	9	4
H-11	6	260	11	9	4	4/14/80	8/13/80	9	4
A-6	7	220	7	10	2	12/18/79	2/07/80	10	2
N-3	7	260	12	7	4	4/16/80	8/13/80	7	4
Total				98	39			95	38

By late in the program we were testing devices from the 260°C ovens on a 2-day cycle, for instance Runs Number 11 and 12 with the Type H-11 and Type N-3 FETs, respectively. Corresponding run times at other temperatures were 10 days at 240°C, 30 days at 220°C, and 90 days at 200°C. Some observations on the testing cycle of biased Type N-3 FETs in particular are given in Section 5.8. Our recommendation for future life test studies is that a pilot run be made with devices of a particular type to help determine an appropriate testing cycle.

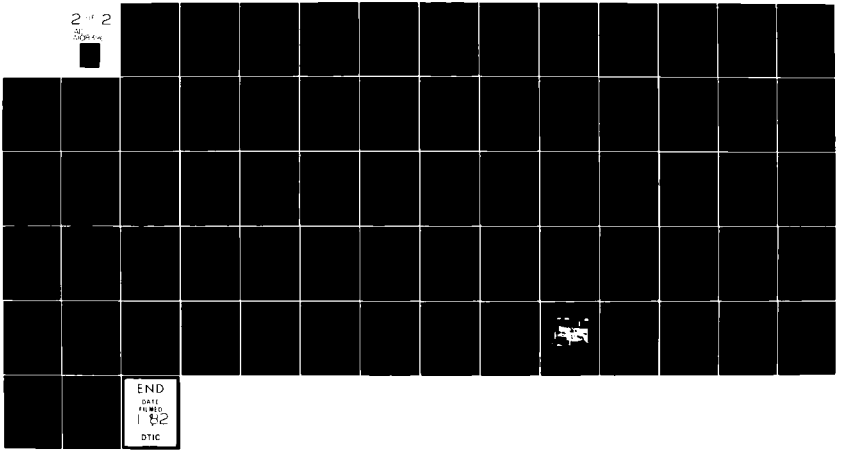
5.3 FAILURE ANALYSIS

Failure criteria for the high temperature constant stress tests were discussed in Section 2.7. As explained there, only the DC failure criteria are used, with the limited RF data affording a means of checking correlation of the RF failure data with the DC failure data. The devices that failed the high temperature constant stress test are indicated in the "No. FETs Failed" column in Table 5-1, which column is rearranged and repeated in Table 5-2. The categories of failure that we have encountered are given in Table 5-2, and the number of biased "B" and unbiased "U" devices that failed in each category is listed. The data came from Table 5-1 and Table A-1.

In many cases, high temperature stress tests were continued on devices after a nominal failure had been recorded. There were several reasons that failed devices were kept under stress. First of all, most devices that are listed as "failed" failed not catastrophically but by exceeding somewhat the specification limits on some parameter, usually the drain current. Thus, the devices were still viable. The failure mechanism was therefore somewhat subtle, and by continuing the high temperature stress test we were able to intensify the causes of degradation failures.

Second, we have noted that frequently a device parameter such as drain current will initially change rapidly and then hold its value within a narrow range. Therefore, if the devices had been subjected to an appropriate initial burn-in procedure, it is likely that the subsequent changes in parameter values might have stayed longer within given specification limits. Thus, by continuing the high temperature stress tests, we were able to gather data on long term parameter changes. We wanted to see if a suitable burn-in procedure to stabilize device parameters before formal life testing begins could

AD-A108 396 HUGHES AIRCRAFT CO TORRANCE CA TORRANCE RESEARCH CENTER F/G 9/1
RELIABILITY INVESTIGATION OF LOW NOISE GAAS FETS.(U)
JUL 81 L S BOWMAN, W YARN F30602-78-C-0295
UNCLASSIFIED HAC-W-43413 RADC-TR-81-181 NL



END
DATE FILMED
1 82
DTIC

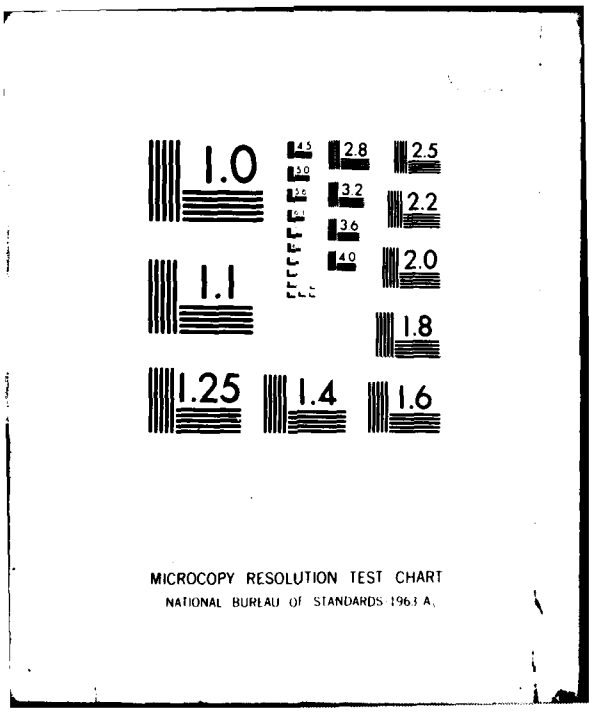

1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

TABLE 5-2

CATEGORIES OF FAILURES IN HIGH TEMPERATURE CONSTANT STRESS TESTS ON CHIP DEVICES

Type Code	Oven No.	Temp °C	Run No.	No. FETs Failed		Temp-Related Failures		Related to Temperature								Independent of Temperature					
								Gate Control		Gate Current		Drain Current		Drain Short		Test/ Handling		Carrier Fracture		Die Attach	
				B	U	B	U	B	U	B	U	B	U	B	U	B	U	B	U	B	U
A-6	7	220	7	10	2	9	2					9	2			1					
	6	240	8	9	4	7	4					7	4					2			
	1	260	9	4	3	4	4					4	4								
A-10	1	260	10	4	2	1	1						1	1		1	1	1		1	
D-1	5	240	6	5	2	4	2					3	2	1				1			
D-2	5	240	6	4	0	4	0					4									
H-1	1	200	2	9	4	6	4	1		1		3	4	1		1		1		1	
	3	220	3	10	4	9	4					9	3		1			1			
H-11	6	260	11	9	4	7	4	3			1	4	3			2					
N-3	2	200	1	10	4	8	3			2		5	3	1		1		1			
	4	220	4	10	4	7	4					6	4	1		2		1			
	7	260	12	7	4	6	3					6	3			1	1				
P-5	6	240	5	4	1	4	1			4					1						
Total				95	38	76	36	4		7	1	60	33	5	2	9	2	8		2	

significantly lengthen the mean time to failure. With the burn-in procedure, not until after the burn-in would the devices be "binned", that is, a relatively narrow set of specifications assigned. Section 5.8 illustrates this idea with the biased Type N-3 FETs.

Third, as but few catastrophic failures occurred as a result of the high temperature stress testing, continued temperature stressing of the remaining FETs would also provide additional information on catastrophic failures.

The temperature stress test is intended to use elevated temperatures to accelerate the failure rates of device types above what they would be at normal operating temperatures. We can then infer the mean time to failure (MTTF) at a given operating temperature using an Arrhenius plot. Therefore, device failures not due to the elevated temperature must be censored before plotting the data. In Table 5-2 the column headed "Temp.-Related Failures" lists the numbers of devices whose failure has been identified as probably due to the elevated temperature of the test. The next four columns of Table 5-2 comprise the categories of failures related to temperature, while the last three columns in Table 5-2 list failures that are not primarily a result of the elevated temperature of the test.

Reference to Table 5-2 shows that, of all FET chips subjected to the high temperature constant stress test, biased devices represented 98/(98 + 39) = 72%. The median number of biased FETs in a test group was 9, whereas the median number of unbiased FETs in a test group was 4. Unfortunately, the small number of unbiased FETs made meaningful comparisons doubtful between test groups. Biased and unbiased FETs of the same device type were stressed at somewhat different temperatures (Section 5.1). They were also subjected to different handling and mechanical stresses, as explained in the next paragraph. Strict comparisons between results on biased and unbiased devices are therefore also difficult to make. For the foregoing reasons, in subsequent discussions of the high temperature constant stress tests the bulk of the results presented will be on biased devices.

An apparent indication in Table 5-2 that the "Carrier Fracture" and "Test/Handling" failure categories seem heavily weighted toward biased devices needs to be explained. Neither of these failure types is directly related to temperature; rather, these failure

types seem directly related to the testing procedures. For instance, as explained in Section 5-1, the alumina microstrip chip carriers of all biased FETs were firmly clamped to the heater block, whereas the unbiased devices were not clamped. Occasionally, during clampdown the thin alumina carrier would fracture. As the unbiased samples were not clamped, this cracking of the alumina ceramic clearly occurred only to biased devices in the high temperature ovens, yet was unrelated to either bias parameters or temperature.

The relatively high incidence of biased device failures in the "Test/Handling" category, compared to unbiased device failures in the same category, is easily explained - the very act of biasing requires additional handling and risk of failure of the biased devices. Thus, the data show a preponderance of biased device failures in the "Test/Handling" category; however, these failures, as those in the "Carrier Fracture" category, are clearly unrelated to either bias parameters or temperature.

Only failures explicitly related to accelerated temperature aging are used to determine the mean time to failure. Before that topic is discussed, however, we examine device degradation.

5.4 DEVICE DEGRADATION

As measurements of DC parameter values were made at regular intervals throughout the course of a test, consistent patterns in parameter changes with time were frequently seen. For example, the drain current of a number of different device types sometimes changed significantly early in the high temperature stress test and then changed much more slowly until the test was terminated or catastropic failure occurred. Such behavior frequently caused the device parameter changes to exceed the preset failure limits relatively early. Subsequent percentage changes in device parameters often remained within the prescribed percentage change limits of Section 2.7 for a considerably longer period of time.

The patterns of parameter changes with time are illustrated in Figures 5-3 through 5-8. We have presented data on biased devices only, in accordance with the discussion in Section 5.3. Figures 5-3 and 5-4 present plots of data on the Type H-1 devices at 200^{o}C

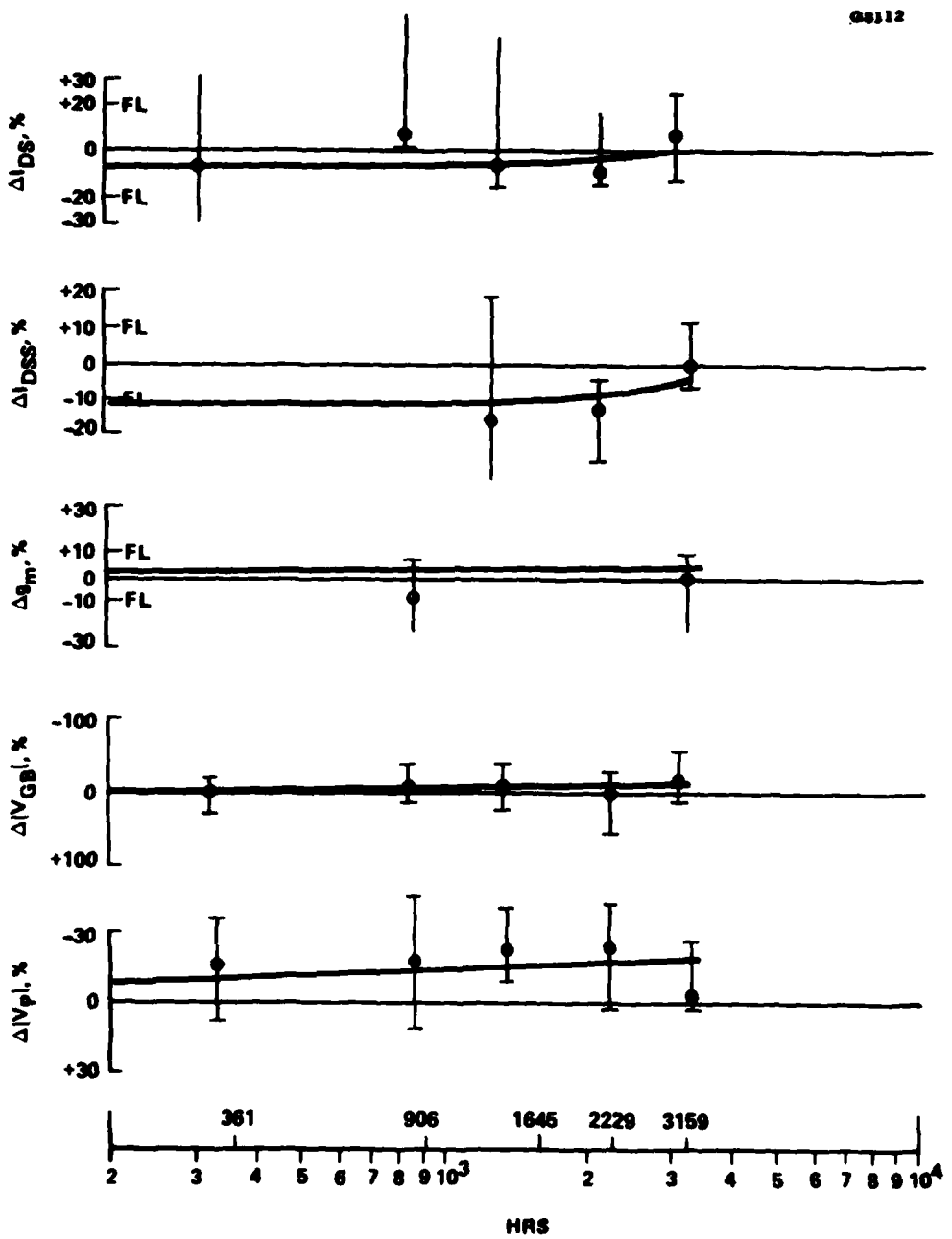


Figure 5-3 Parameter changes with time for biased H-1 FETs at 200°C.

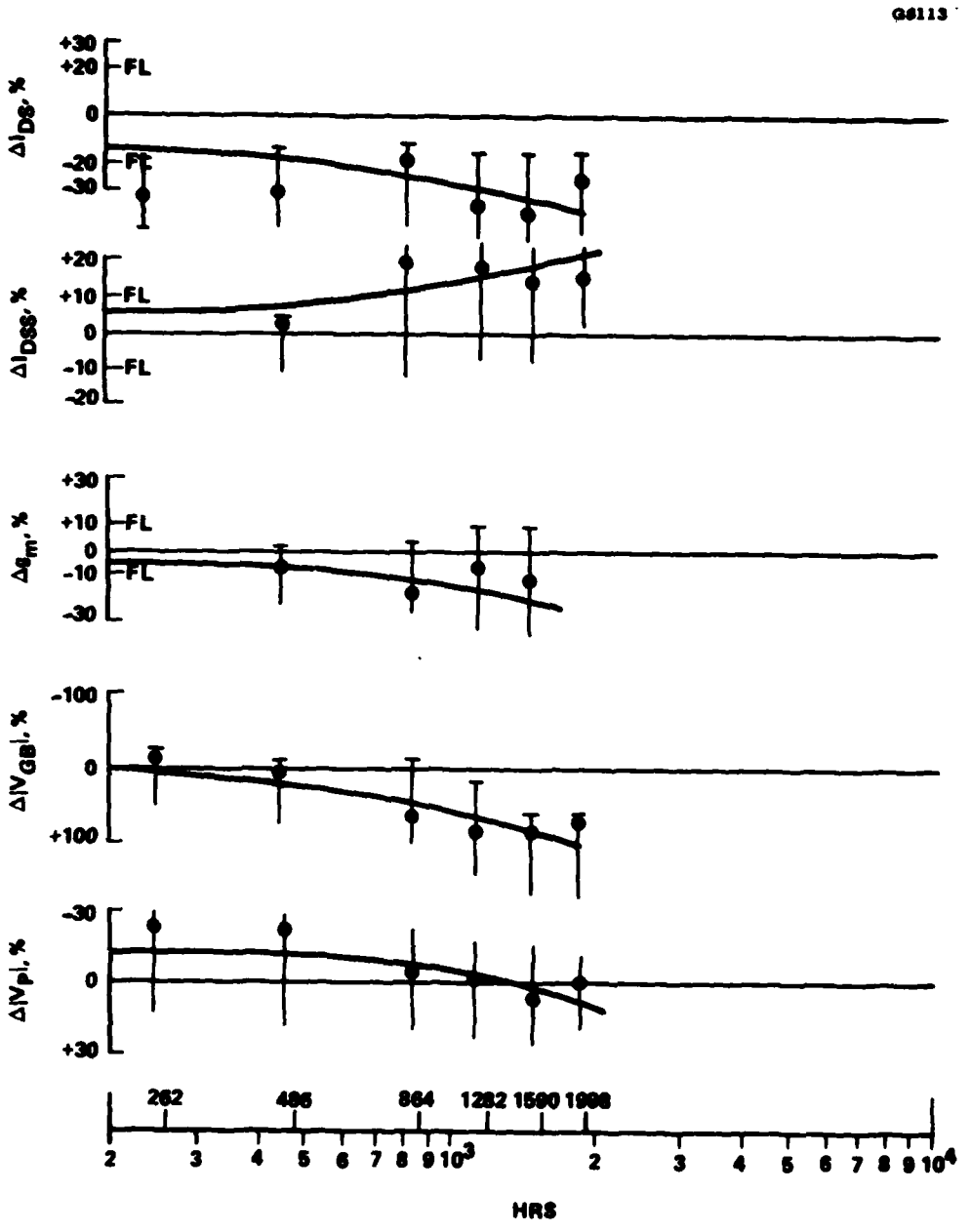


Figure 5-4 Parameter changes with time for biased H-1 FETs at 220°C.

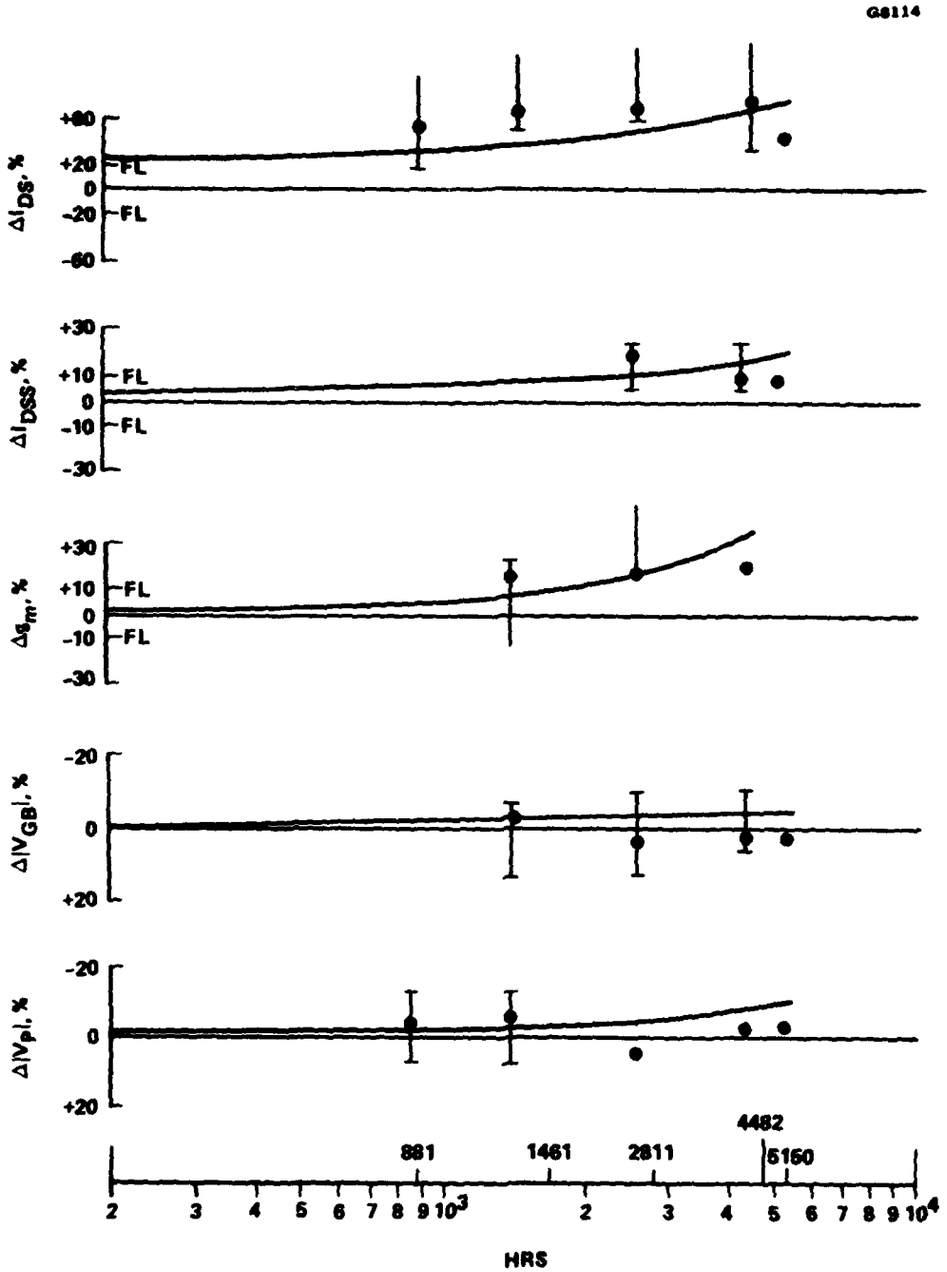


Figure 5-5 Parameter changes with time for biased N-3 FETs at 200°C.

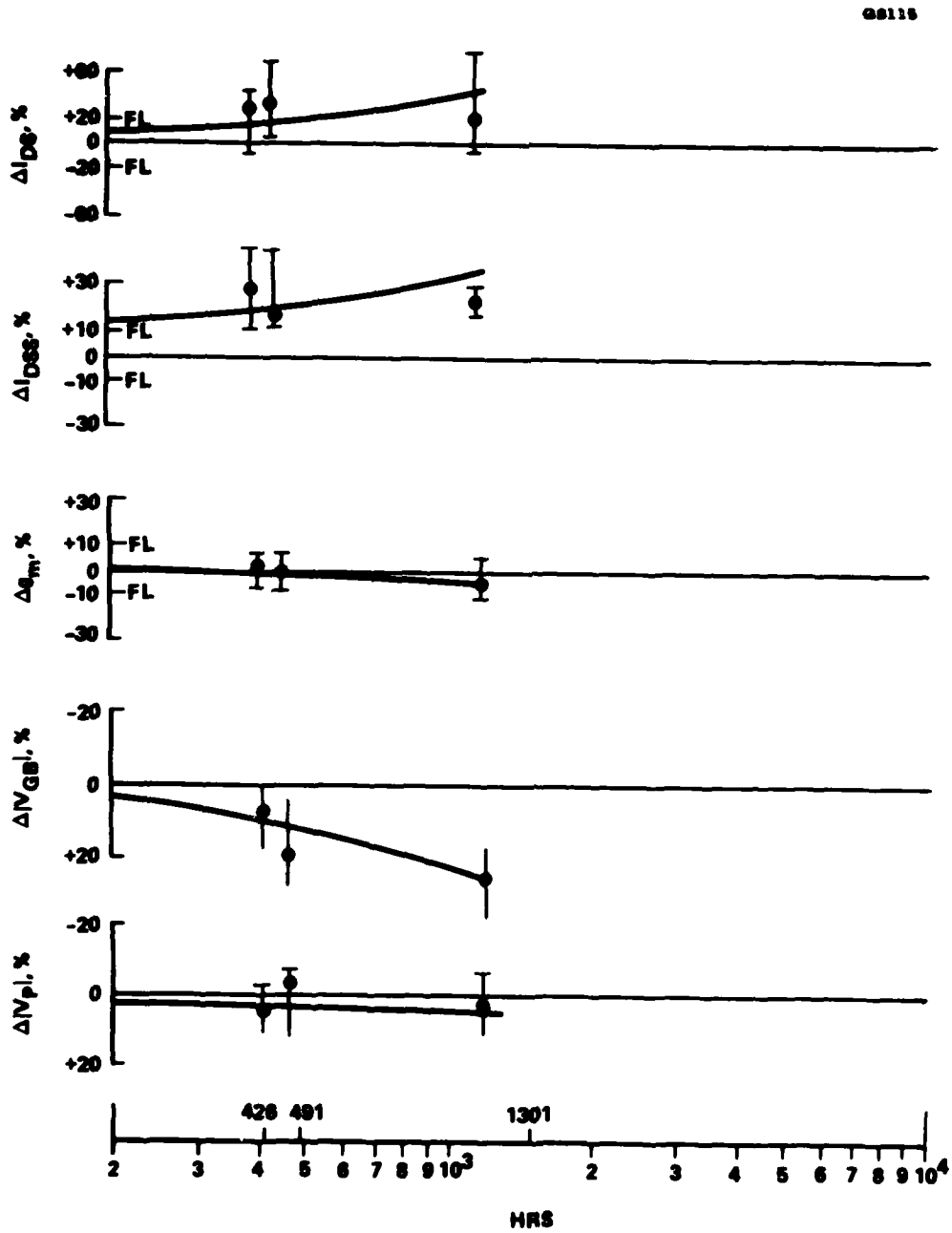


Figure 5-6 Parameter changes with time for biased N-3 FETs at 220°C.

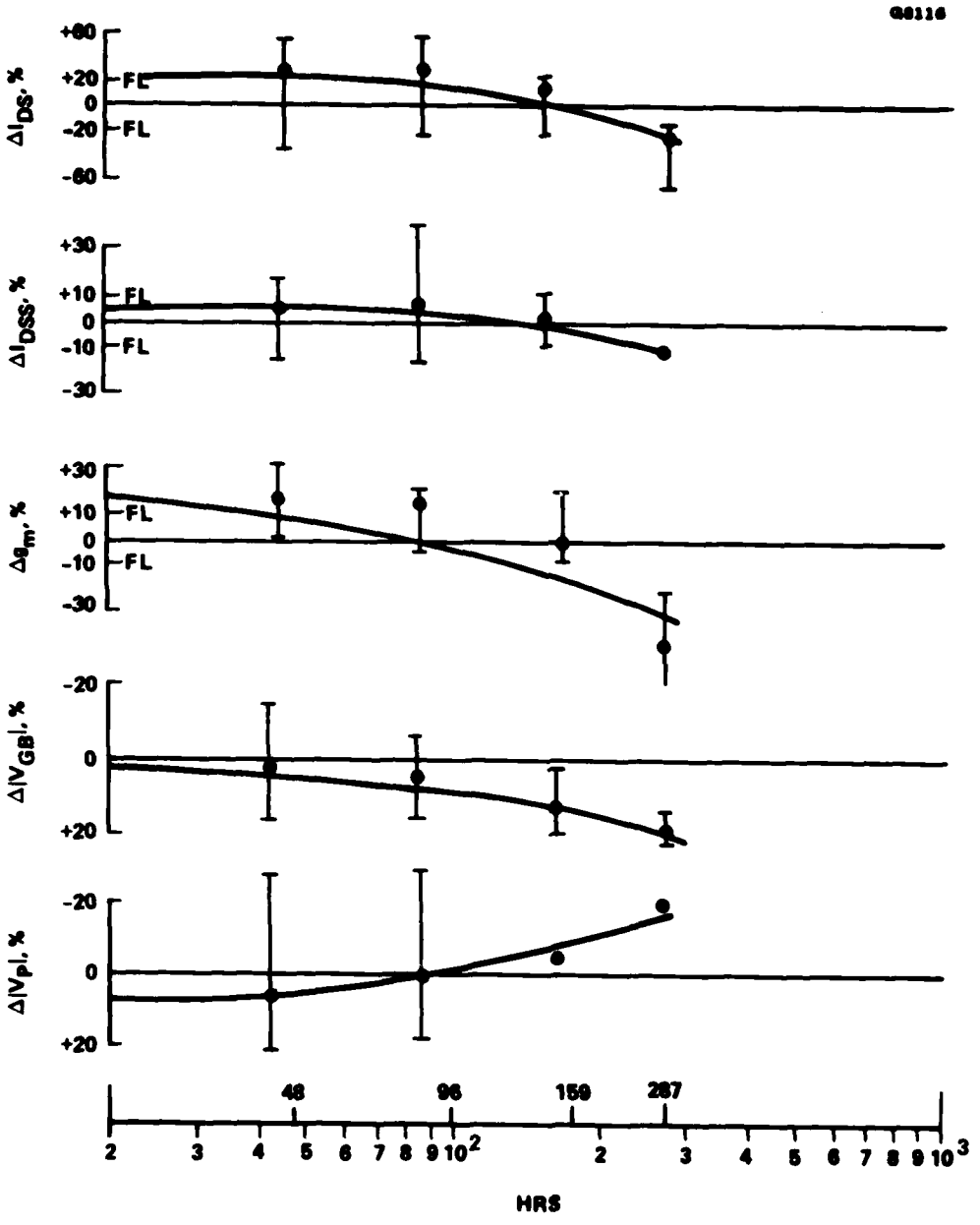


Figure 5-7 Parameter changes with time for biased N-3 FETs at 260°C.

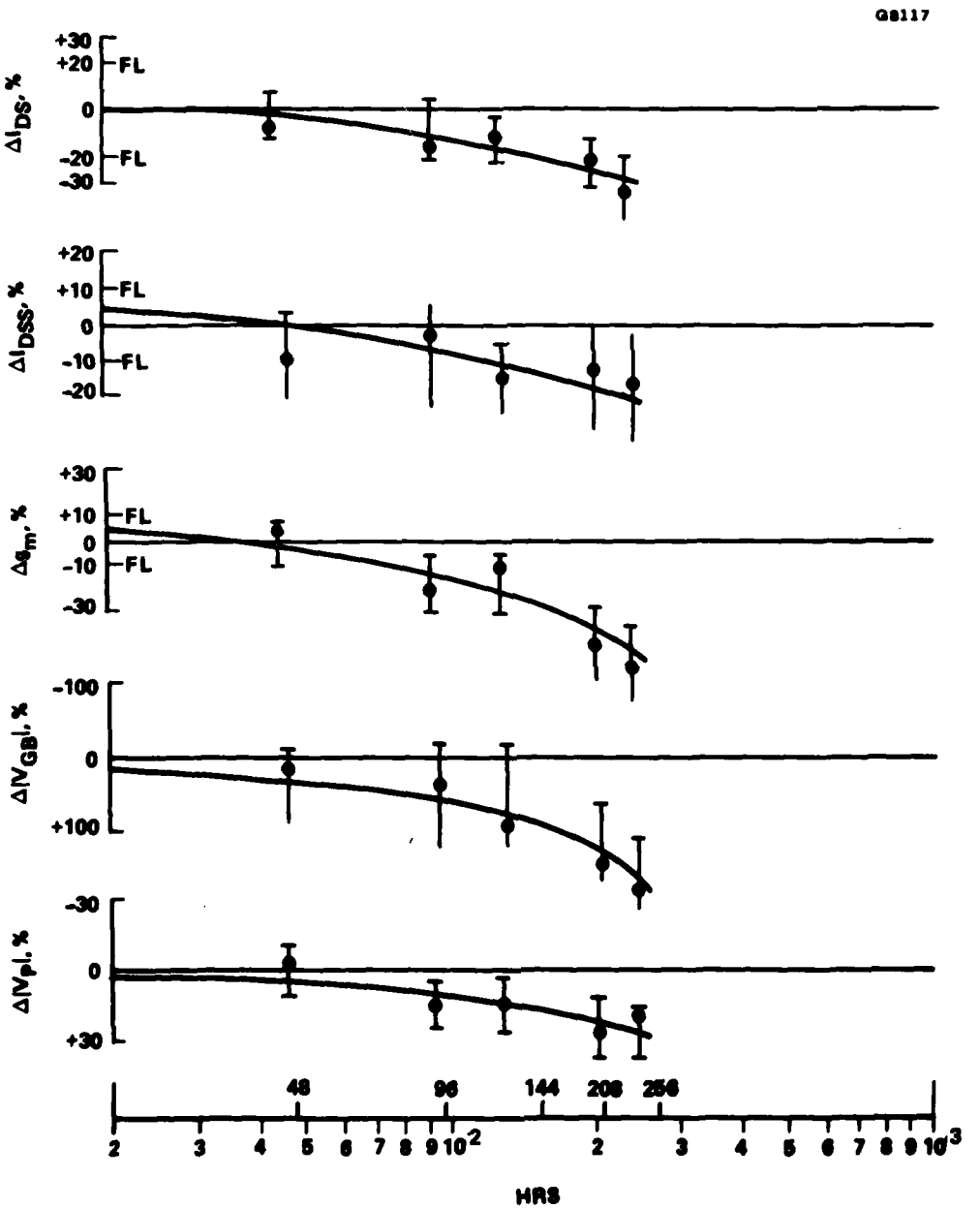


Figure 5-8 Parameter changes with time for biased H-11 FETs at 260°C.

and 220°C, respectively. Figures 5-5, 5-6, and 5-7 illustrate the behavior of the Type N-3 devices at 200°C, 220°C, and 260°C, respectively. Note the change of abscissa scale by a factor of 10 in Figure 5-7 for devices tested at 260°C. The scale change was made to accommodate the graphs to the extremely rapid aging characteristics of FETs at 260°C. Finally, Figure 5-8 shows plots of the Type H-11 devices at 260°C with the same abscissa scale as Figure 5-7.

In Figures 5-3 through 5-8 plots are made of the three important DC parameters that are given along with their prescribed failure limits in Table 2-8. On the ordinate scale of these three plots, the designation "FL" indicates the specified failure limits. Also included in Figures 5-3 through 5-8 for completeness are plots of percentage changes in the magnitudes of the low noise gate bias and the gate pinchoff voltage. In these plots the median of the data at a measurement time is indicated by a solid circle. Vertical bars with horizontal tic marks indicate the range of measured values.

A linear regression analysis (LRA) for each plot was performed for the median data points, plus a defined ordinate value of zero at initial time. The results of the LRA are the smooth curves shown on the plots. Because of the logarithmic abscissa scale, the LRA lines appear curved.

Except for the plot of Δg_m in Figure 5-7, the LRA line of the g_m values at initial time fell well within the 10% failure limits prescribed for this parameter and typically was near zero. However, in the case of the drain current parameters ΔI_{DS} and ΔI_{DSS}, the LRA line at initial time typically fell near the failure limits or even exceeded them. The median data points, except for the initial measurement, tend to be grouped somewhat in a horizontal pattern. This observation leads one to the conclusion that the early drain current measurements, say those for under 168 hours, might be disregarded and a new "zero" established after a week's burn-in.

The typical consequences of this action would be that the LRA line would now extrapolate back to near zero, and the projected mean time to failure for causes related to changes in drain current would be significantly increased. Therefore, if the FETs had been given an initial burn-in to stabilize the devices prior to setting "initial" values of the parameters from which percentage changes would be measured, it is

possible that the drain current on many devices would have stayed within specification longer. As a matter of interest, Table 5-2 shows that the vast majority of temperature induced failures, that is, (60 + 33)/(76 + 36) = 83%, occurred when the drain current exceeded the specification limits. The drain current values frequently exhibited the behavior of rapid change followed by gradual change described in the first paragraph of this section. Thus, because of the overwhelming influence of the drain current "failures" on the total temperature-related failure results, the overall projected degradation failure rate of a FET type may be significantly shorter for FETs with no burn-in period.

We recognized the importance of an initial burn-in period at the outset of the program. We were also well aware that standard industry practice included a burn-in period for newly obtained devices before they were committed to service. However, as we felt that the purpose of the reliability study was to test the FETs from the outset, we waived both incoming inspection and initial burn-in considerations. The point of this discussion is to make the reader aware that the Mean-Time-To-Failure (MTTF) results shown in this report will probably be significantly less than would be obtained following standard industry inspection and conditioning procedures.

5.5 FET SELECTION FOR RELIABILITY ANALYSIS

Further discussion is in order, regarding MTTF expectations in actual field use of microwave low-noise FETs. Because of the huge cost involved in procuring sufficient numbers of FETs for obtaining accurate statistical projections of lifetime performance, we chose to concentrate our efforts on three selected device types. In the "Initial Inventory (Chip)" column of Table 2-1 are listed the original numbers of devices procured for the program. To form the backbone of the investigations, major acquisitions were made of only the following FET chip types:

A-1: 50 units (replaced by Type A-6, 50 units)
H-1: 76 units (replaced by Type A-11, 15 units)
N-3: 61 units

Type A-1 FETs were wholly unusable because of a metallization problem, as was discussed in Section 3. These FETs were replaced with Type A-6 FETs on a one-for-one basis by the supplier. However, at the times that we first cooled each of the three ovens containing the Type A-6 FETs to measure their parameters, all devices were found to have failed. Thus, no statistics could be obtained at any of the three test temperatures on this type device. The failure mode was felt possibly to be related to an undesired compensation of the channel doping. A discussion of the failure of Type A-6 FETs is given in the Final Report of the Failure Mechanism Program.[1] Thus, the extensive work with the 50 Type A-1 devices and with the 50 Type A-6 devices yielded little usable reliability information.

A different set of problems was encountered with the Type H-1 FETs. First of all, our operators had difficulty wire bonding to the Type H-1 chips, as the dice fractured frequently. Second, at the test temperatures, the devices were found to form an intermetallic gold-aluminum alloy in the gate region. The formation of the intermetallic alloy was the principal observable failure mode. Further discussion of the Type H-1 FET failures is given in the Final Report of the Failure Mechanism Program.[1] The supplier was contacted, and he informed us that the Type H-1 FETs were being replaced by the Type H-11 FETs. We were sent 15 Type H-11 FETs for testing. Because the Type H-1 FETs were now obsolete, we cancelled plans to test these devices at a third temperature and left 22 devices uncommitted (Table 2-1). As a consequence of these considerations, limited statistical data were obtained on Type H-1 devices. We did test the Type H-1 FETs at 200°C and at 220°C. MTTF data on the Type H-1 FETs are presented in Section 5.6.

As these device results are unfolded, the reader should keep continually in mind that the Type H-1 devices have been replaced by the Type H-11 devices. Test results of the Type H-1 FETs at 200°C and at 220°C, as shown in Figures 5-3 and 5-4, can be compared with test results shown in Figure 5-8 on the Type H-11 FETs, keeping in mind that the Type H-11 FET results were obtained at 260°C. The improved Type H-11 FETs show in Figure 5-8 a much more consistent pattern of parameter changes with time, with regard to the means, ranges, failure limits, and LRA lines, including slopes and intercepts. MTTF data on the H-11 FETs are presented in Section 5.6.

The remaining FET chip that we procured in relatively large numbers was the Type N-3. We had no real difficulties with this type FET and were able to place 40 devices on test in the high temperature ovens at three different temperatures. Sufficient numbers of devices were used to give meaningful statistics. Preliminary losses of the Type N-3 FETs were so low that we were able to accomplish our test goals and still retain a contigency reserve of 15 devices uncommitted. Results of our measurements are plotted in Figure 5-5 for 200°C tests, Figure 5-6 for 220°C tests, and Figure 5-7 for 260°C tests.

MTTF data and an Arrhenius plot on the Type N-3 FETs are presented in Section 5.6. The comments made earlier in this section about changes in the drain current parameters apply to the Type N-3 FETs. Consequently, the MTTF values appropriately can be considered to be smaller than those expected for Type N-3 devices actually placed into service in a well-designed system. Of uppermost importance is also the fact that we purchased the lowest reliability grade of devices from this supplier. With three higher reliability grades of devices available, the systems designer can usually specify Type N-3 FETs having the needed reliability grade.

5.6 MEAN TIME TO FAILURE

The purpose of accelerated temperature stress testing is to determine the mean time to failure at temperatures considerably higher than normal operating temperatures and then to extrapolate the results to predict the mean time to failure under normal service. The numbers of FET failures attributable to temperature effects are shown in four columns of Table 5-2 and are totaled in the column titled "Temp. - Related Failures" in the same table. Table 5-3 shows the hours of FET operation until discovery of a temperature-induced failure in high temperature constant stress tests on chip devices. The column headed "Temp. - Related Failures" in Table 5-2 is repeated under the heading "N" in Table 5-3. Data on failed devices from a specific run were arranged in ascending order of hours to failure, using the data of Table A-1. These hours, along with the ordinal number of the failed FET in both the biased and unbiased categories, are shown in Table 5-3. Figure numbers of corresponding plots are also shown in Table 5-3.

TABLE 5-3

HOURS OF FET OPERATION UNTIL DISCOVERY OF A TEMPERATURE-INDUCED FAILURE IN HIGH TEMPERATURE CONSTANT STRESS TESTS ON CHIP DEVICES

Type Code	Oven No.	Temp °C	Run No.	N		Ordinal Number of Failed Biased FET									Figure No.	Ordinal Number of Failed Unbiased FET				Figure
				B	U	1	2	3	4	5	6	7	8	9		1	2	3	4	
A-6	7	220	7	9	2	1223	1223	1223	1223	1223	1223	1223	1223	1223		1223	1223			
	6	240	8	7	4	1276	1276	1276	1276	1276	1276	1276				1276	1276	1276	1276	
	1	260	9	4	4	533	533	533	533							533	533	533	533	
A-10	1	260	10	1	1	163										163				
D-1	5	240	6	4	2	1095	1095	1095	1095							1095	1095			
D-2	5	240	6	4	0	1095	1095	1095	1095											
H-1	1	200	2	6	4	361	361	907	907	1645	3159				5-9	361	361	361	361	
	3	220	3	9	4	263	263	263	263	263	263	263	263	263		263	846	1282	1282	5-10
H-11	6	260	11	7	4	48	96	96	96	144	144	144			5-11	48	48	96	96	
N-3	2	200	1	8	3	599	881	881	881	881	881	881	2812		5-12	881	1465	1465		
	4	220	4	7	4	65	426	426	426	426	426	1301			5-13	426	426	426	426	
	7	260	12	6	3	48	48	48	48	48	48				5-14	48	48	48		
P-5	6	240	5	4	1	318	318	318	318							24				

From Table 5-3 a log-normal plot can be made for each temperature and device type, where the ordinate is the time to failure and the abscissa is the percentage of failures up to that time, with the denominator for the percentage calculation being one greater than N, which is the number of devices in the sample. The mean time to failure (MTTF) is the time corresponding to the 50% point on the abscissa. Theory predicts that the data points will fall on a straight line, if the abscissa scale is "normal" and the ordinate scale is logarithmic.[4]

As the data points typically exhibit considerable scatter, a least squares line should be drawn on the log-normal plots, provided three or more distinct data points are available. Figures 5-9 through 5-13 show log-normal plots of the data from Table 5-3, including approximate least squares lines.

A few words of discussion are necessary on a least squares approximation, where fewer than four data points are available. In these plots not only the vertical position, but also the slope of the straight line has significance, and four or more data points are required to give confidence in the slope of the least squares line. Therefore, Figure 5-9 with four data points allows a least squares line to be drawn with some confidence in the slope. A line with that same slope has been drawn on Figures 5-10, 5-11, 5-12 and 5-13, approximately to minimize the least squares distances to the three data points in each of these four figures. With the available data, we feel that this approach is the best for obtaining reasonable approximations to the mean time to failure of these devices. The mean time to failure (MTTF) is the ordinate value corresponding to the 50% point on the abscissa. Interpretation of the results should be undertaken with due regard to the discussions in Sections 5.4 and 5.5.

No log-normal plot is drawn for devices in Table 5-3 that have only one or two separate data points. Therefore, device types H-1, H-11, and N-3 have log-normal plots in this report. These are the device types that were selected for program emphasis, as was explained in the previous section. Only the biased type N-3 FETs have plots at two temperatures, and from Figures 5-12 and 5-13 the MTTF values are found to be 600 hours at 200°C and 160 hours at 220°C. In the next two paragraphs we make some inferences concerning the MTTF of biased Type N-3 devices at 260°C. Additional discussion of the MTTF of the biased Type N-3 devices is given in Section 5.8.

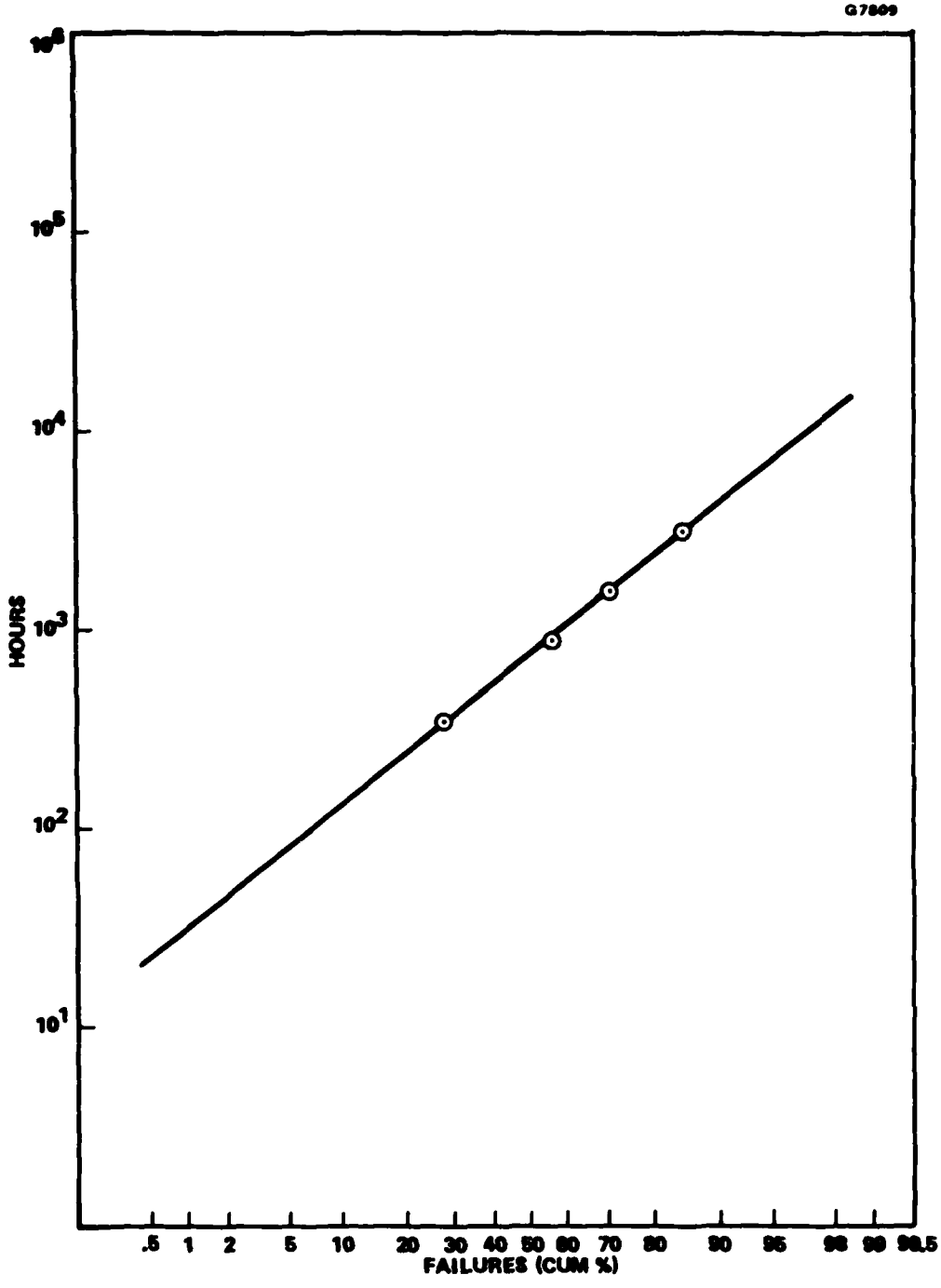


Figure 5-9 Log-normal plot for biased H-1 FETs at 200°C.

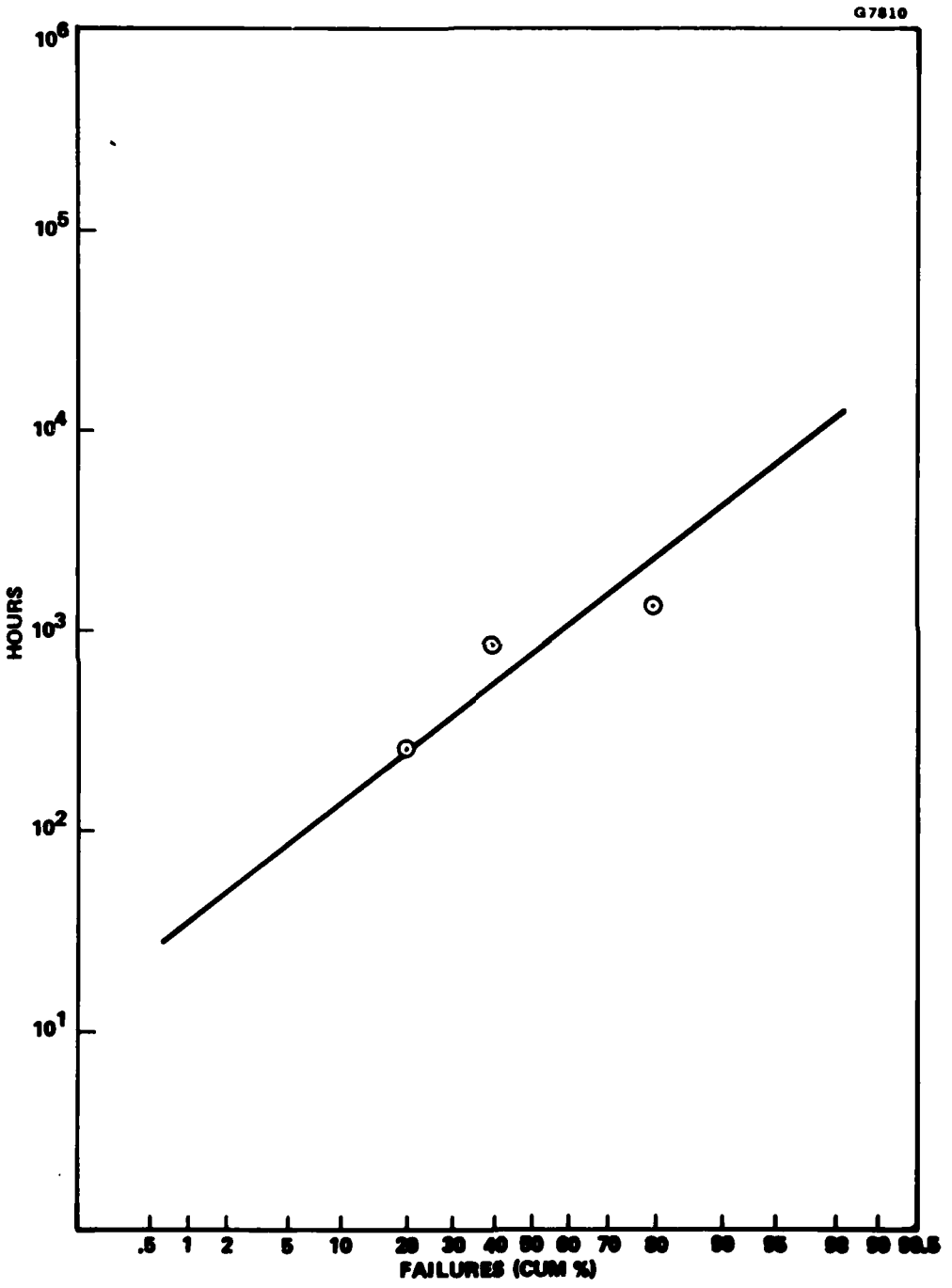


Figure 5-10 Log-normal plot for unbiased H-1 FETs at 220°C.

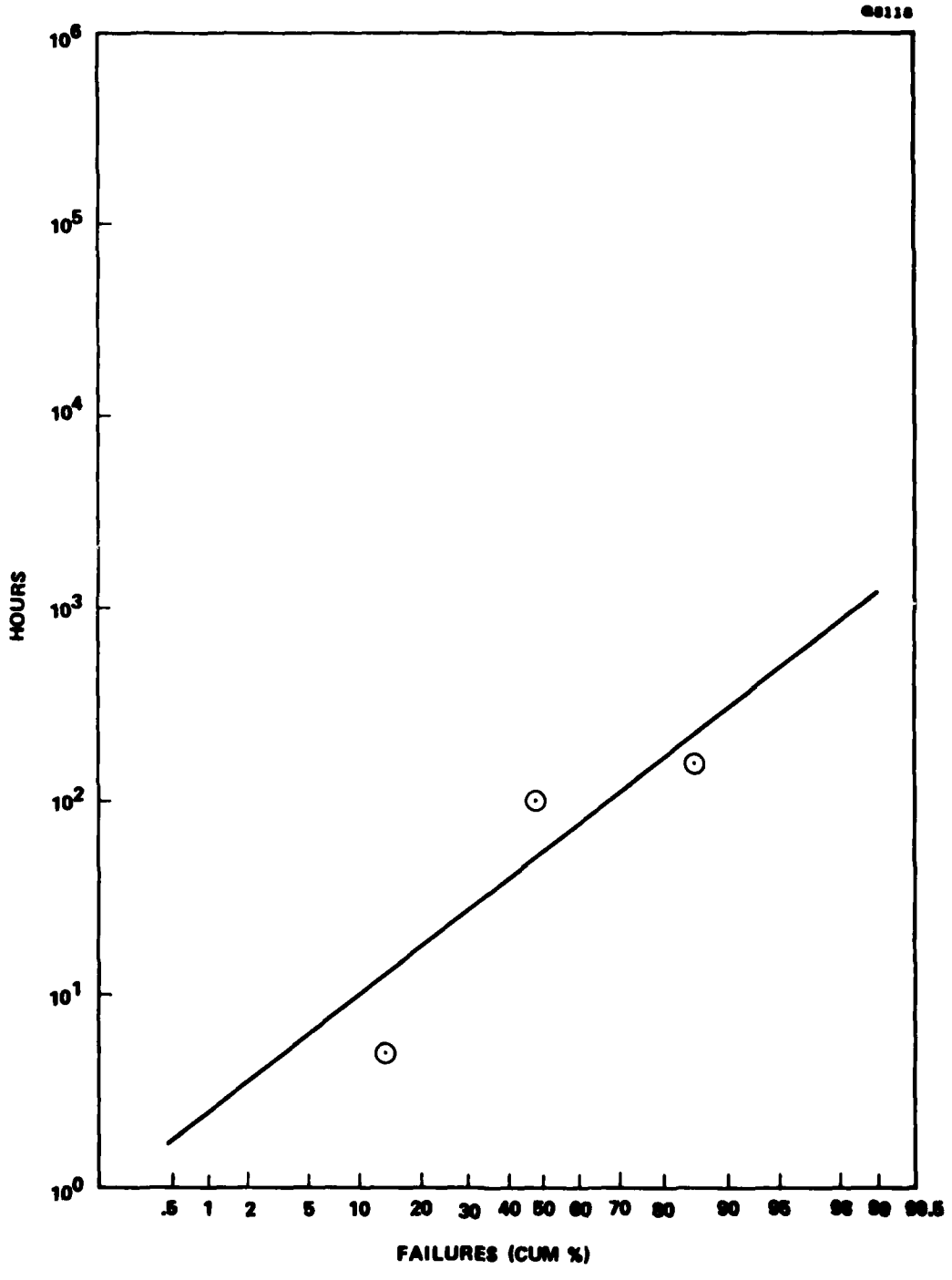


Figure 5-11 Log-normal plot for biased H-11 FETs at 260°C.

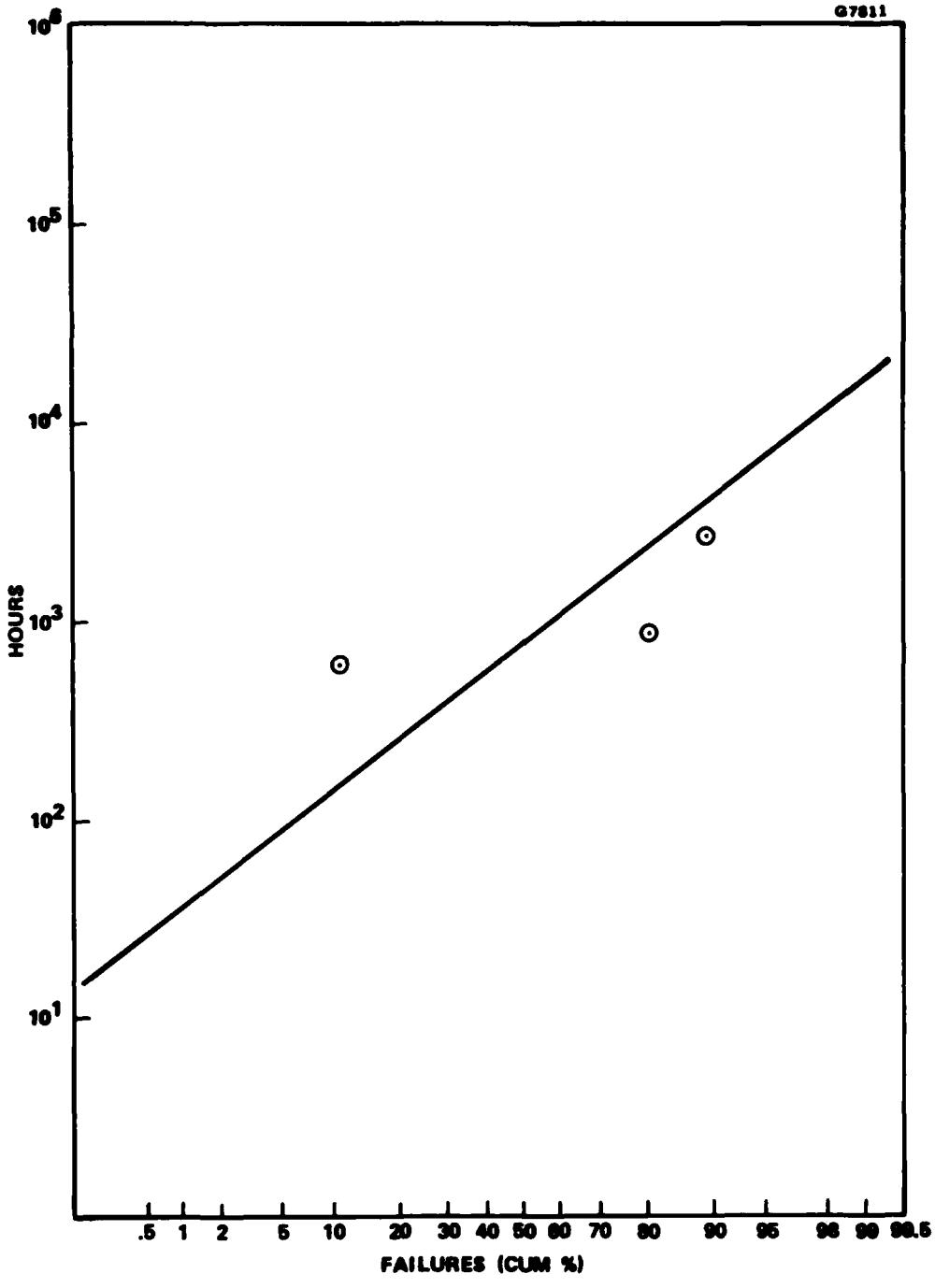


Figure 5-12 Log normal plot for biased N-3 FETs at 200°C.

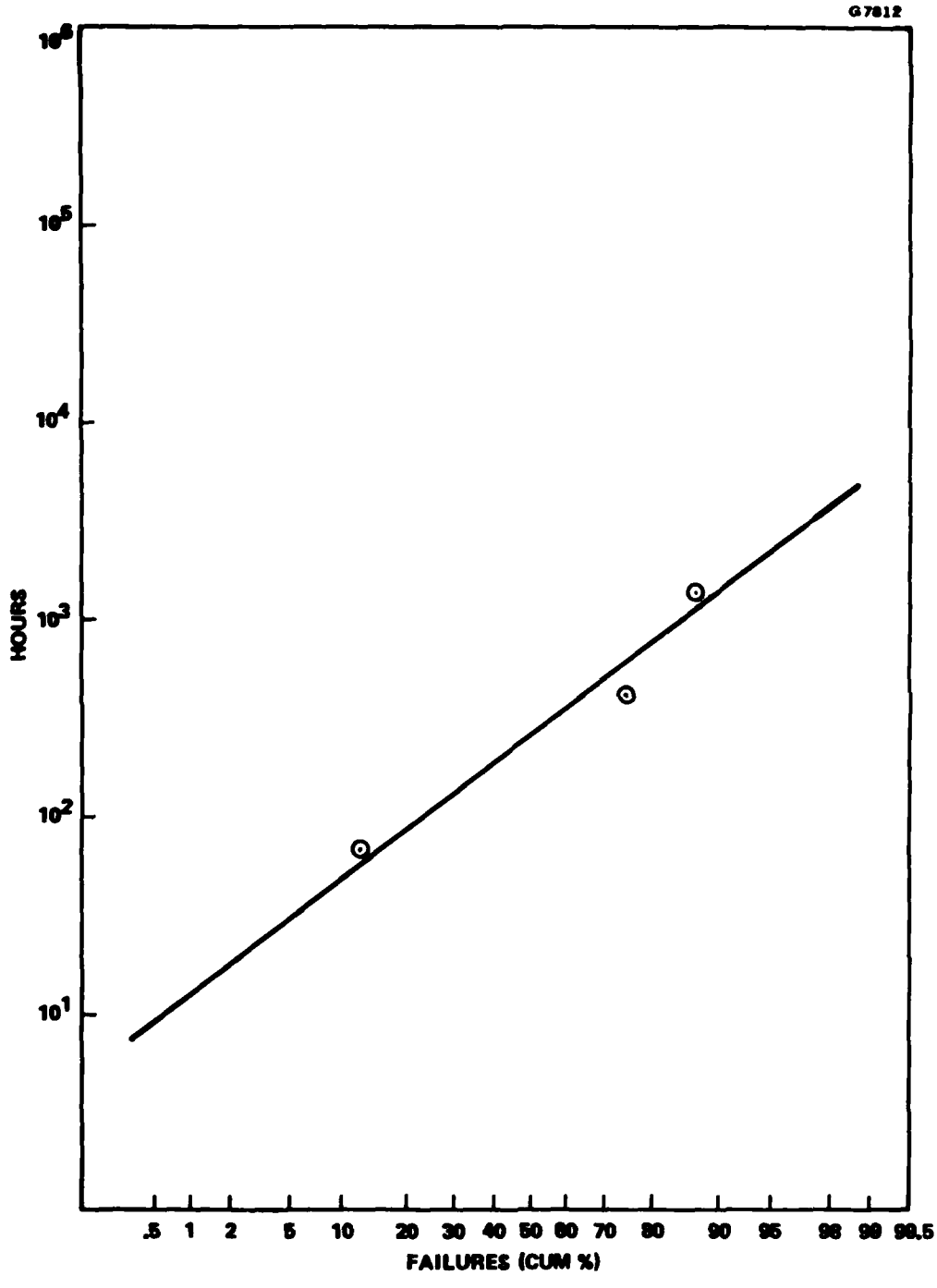


Figure 5-13 Log-normal plot for biased N-3 FETs at 220°C.

For Run Number 12 the data of Table 5-3 show that all six temperature-induced failures of Type N-3 FETs stressed at 260°C had occurred by the time that 48 hours had elapsed and we made our parameter measurements. These failures were all due to the drain current readings going out of specification. However, as shown in the data sheets from which Table A-1 was compiled, the drain current readings for Device Number 145 from the same group were still within the specification limits of Table 2-8 after 96 hours at 260°C stress. Unfortunately, the device was destroyed in a handling accident before parameter measurements could be made at 159.6 hours. Table 5-4 shows the measured values of specific drain current changes with time for the seven biased Type N-3 FETs of Run Number 12, along with the allowable failure limits from Table 2.8.

We know, therefore, even in the worst case assumption that Device Number 145 might have failed immediately after the 96 hour time point, that one FET of the seven survived 96 hours at 260°C. Following the standard procedure for calculating the cumulative percentage of failures for a log-normal plot[4], we obtain one conservative data point of 87.5% cumulative failures after 96 hours of 260°C stress. On log-normal coordinates a straight line through this data point having the same slope as the corresponding lines in Figures 5-12 and 5-13 yields an MTTF value of 12 hours at 260°C. The three values of MTTF will be used in the next section to make an Arrhenius plot for biased Type N-3 FETS.

5.7 ARRHENIUS PLOT

Many failure mechanisms in semiconductor technology have been found to obey the Arrhenius equation, which states that the chemical reaction rate is proportional to $\exp(-E_A/kT)$, where E_A is the activation energy, k is Boltzmann's constant, and T is the absolute temperature.[4] If the failures of a semiconductor device type stressed at several different elevated temperatures arise from the process described, then the mean-time-to-failure (MTTF) can be plotted as a function of temperature, and the graph can be extrapolated to predict the MTTF at normal operating temperatures. In this report an Arrhenius plot is a plot of the logarithm of the MTTF versus reciprocal absolute temperature. Theory predicts a straight line for this choice of axis scaling. The activation energy for the specific failure mechanism is proportional to the slope of the straight line.

TABLE 5-4

MEASURED VALUES OF DRAIN CURRENT AS A FUNCTION OF TIME FOR THE SEVEN BIASED TYPE N-3 FETs OF RUN NUMBER 12 AT 260°C

Serial Number	I_{DS}, mA				
	0 hrs	48 hrs	96 hrs	159.6 hrs	207.6 hrs
144	15	19			
145	17	20	14	Destroyed	
147	22	28			
148	20	29	30	20	7
150	20	25	23	22	
153	20	25	25	17	9
154	19	25	25	23	13

Figure 5-14 is an Arrhenius plot of the three MTTF values obtained in Section 5-6 for the biased Type N-3 chip devices. The equivalent degrees Centigrade are shown on the reciprocal absolute temperature scale. A least squares line is also shown for the three data points. As explained in the previous section, the placement and slope of the line in Figure 5-14 should be viewed with some skepticism, as the MTTF at a fourth temperature in unavailable. Nevertheless, extrapolating the line in Figure 5-14 to operating temperatures indicates an estimated MTTF of biased Type N-3 devices at $100^{o}C$ of the order of 10^{7} hours. If a single failure mechanism is postulated for the Type N-3 biased devices, the activation energy is approximately 1.5 eV.

5.8 THE EFFECTS OF TEST DESIGN

The Arrhenius plot of Figure 5-14 was obtained on devices that were neither pre-tested nor burned-in. As discussed in Sections 5.3 and 5.4, we kept devices on test past their nominal failure point, with the idea in main that specification of an initial burn-in period might increase the MTTF. An initial burn-in if used, would be expected to stabilize the drain current values at somewhere near the maximum values shown in Table 5-4. A proper burn-in period would likely not be 48 hours at $260^{o}C$, but as short a time as is needed at a considerably lower temperature.

Reference to Table 5-4 shows, if an appropriate burn-in period is used, that the devices would tend to last some 150 hours at $260^{o}C$. True degradation tends to occur well after 100 hours of stress, which is an order of magnitude greater than that found in Section 5.6 for these devices. This observation leads to the conclusion that the MTTF values obtained from Figure 5-14 may be understated by as much as an order of magnitude, because of the test design. Thus, the operational MTTF for many applications may be as high as 10^{8} hours.

Other peculiarities of the test design also emerge from the data of Table 5-4. For example, if our measurement interval had been a week instead of two days, many of the devices would have been found still within specification. What would have happened, of course, is that we would have missed seeing the drain current increase initially. Then, as the drain current degraded again, we would have thought that little had changed. The "measured" MTTF would have turned out to be much larger!

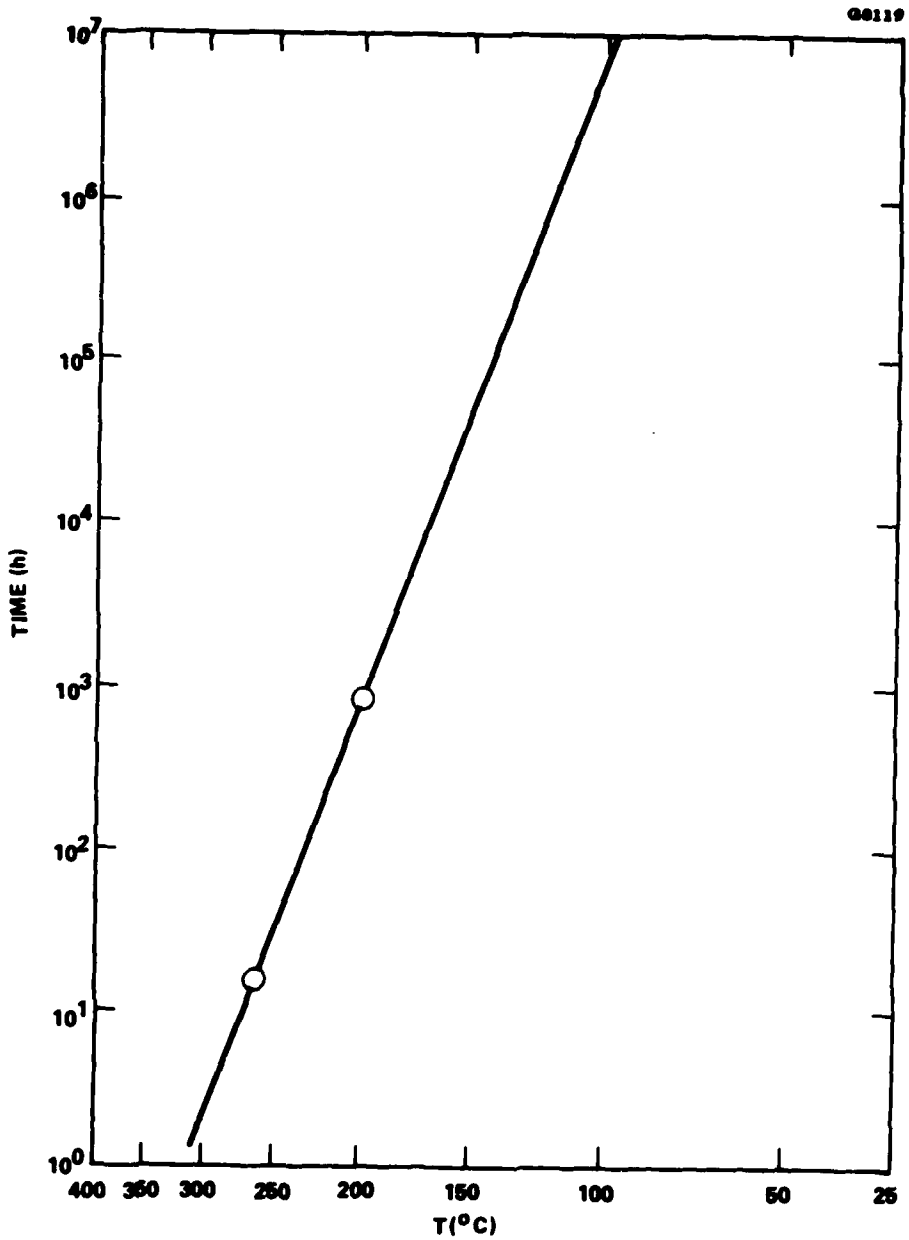


Figure 5-14 Arrhenius plot of biased type N-3 devices.

Also, the ±20% specification on ΔI_{DS} was not firmly grounded in a system requirement. It is interesting to note from the data of Table 5-4, if the specification had been relaxed to ±30% or merely to ±25%, that a significant number of devices would have remained within specification much longer. Thus, to be of maximum usefulness, a life testing program should be tied intimately to system requirements.

These conclusions were reached using the results on the biased Type N-3 FET chips stressed at 260°C. However, examination of the data on other devices suggests that conclusions along similar lines would be reached for them also.

5.9 RF AND S-PARAMETER TEST DATA

Devices that were subjected to the high temperature constant stress tests were given RF and S-parameter measurements. Details of these measurements are discussed in Section 2.5 and 2.6. RF failure criteria from a previous program[2] are given in Section 2.7 and consist of an increase in the minimum noise figure by 0.5 dB or a decrease in associated gain of 1 dB near 10 GHz. No failure criteria were specified for the S-parameter measurements.

Measurements were made on 100% of the devices initially and on all remaining devices when an oven was shut down. During the course of the tests, measurements were made on a small sampling of the FETs under test. As shown in Tables 5-1 and 5-2, by the end of the testing period almost all devices had failed the DC criteria, yet were still viable. Our purpose in this section is to compare the initial and final values of the minimum noise figure and associated gain. We also discuss the S-parameter measurements. The device types selected for discussion in this section are the same types that were principally studied in Sections 5.6 and 5.7, namely, the Type H-1, H-11, and N-3 FETs.

Table 5-5 gives representative measurements of the initial and final values of minimum noise figure and associated gain near 10 GHz. The data seem to indicate that the noise figure sometimes decreased over time and that sometimes the associated gain increased. These observations are not to be interpreted literally. Because devices were not initially inspected, screened, and burned-in, the initial measurements may not necessarily represent the minimum noise figure. Nor were the devices necessarily

TABLE 5-5

REPRESENTATIVE MEASUREMENTS OF INITIAL AND FINAL VALUES OF MINIMUM NOISE FIGURE AND ASSOCIATED GAIN NEAR 10 GHz

Run No.	Temp °C	FET Type	Biased/ Unbiased	Device No.	Initial, dB		Final, dB		Final Hours
					F_{min}	G_a	F_{min}	G_a	
2	200	H-1	B	25	4.20	5.80	5.41	2.74	3159
3	220	H-1	U	34	5.00	4.07	3.78	5.44	1998
3	220	H-1	U	42	6.10	4.20	4.59	3.49	1998
4	220	N-3	B	49	2.86	7.95	2.99	8.25	1300
4	220	N-3	B	51	2.59	8.60	2.89	8.85	1300
11	260	H-11	B	172	3.75	6.20	4.49	5.27	256
11	260	H-11	B	181	5.24	3.73	4.55	5.02	256
12	260	N-3	B	148	3.18	8.08	4.11	7.46	208
12	260	N-3	B	150	2.92	9.20	2.87	8.45	208
12	260	N-3	B	153	2.96	9.18	3.66	8.25	208
12	260	N-3	B	154	3.85	7.20	3.86	6.79	208

designed for minimum noise figure near 10 GHz. As the FETs aged, we know that the DC parameters changed and suspect that the RF characteristics in some instances could also have changed such that the minimum noise figure at 10 GHz could have decreased, while the absolute minimum noise figure over the operating band might have increased. Our data are insufficient to resolve this question. Parallel tracking of the DC and RF parameter changes will be obtained to a limited extent in the RF constant stress test that is discussed in Section 7.

Some answers to the questions of RF parameter changes over the 2 to 12 GHz range could be answered by analyzing sufficient S-parameter data. However, having taken S-parameter measurements on a sampling basis, we also have insufficient S-parameter data on specific devices to obtain definitive answers.

Therefore, on this program we were unable to resolve the question of correlation between DC and RF parameter changes. This conclusion is consistent with our orientation that this was an extensive program, where many devices would be tested, rather than an intensive program requiring in-depth studies of a few selected device types. Intensive programs would require large numbers of specific device types and sufficient tests to assign a high confidence level to the conclusions.

In an intensive type program, it would be vital at the beginning to designate certain devices having known characteristics as benchmark standards for checking calibration of the test equipment and methods and against which the devices being tested could be compared. With the great diversity of device types and quite limited numbers of each on the present program, using benchmark devices was considered not to be feasible. We relied on the calibration of equipment and competency of the operators to assure accuracy and repeatability. Qualitative comparisons of our findings furnished an internal means of checking consistency and giving confidence in the results.

Although we have collected considerable amounts of S-parameter information from 2 to 12 GHz, except for designing the amplifier matching circuits for the RF stress tests, no direct use was made of the S-parameter data on this program. Consequently, S-parameters are not emphasized in this report.

Table 2-7 gave typical initial measurement of S-parameters at 6 GHz for the low noise FET devices tested on this program.

Taking RF and S-parameter data on a large number of devices generates an impressive collection of numbers for later analysis. It is the strong recommendation of the authors that automated testing and data collection and handling methods be an integral part of future programs, wherever possible.

6.0 MEDIUM TEMPERATURE CONSTANT STRESS TESTS ON PACKAGED FETs

6.1 TEST APPROACH

Medium temperature constant stress tests on packaged FETs have been carried out at 85°C and 120°C in a manner similar to those on the chip FETs, except that the protective atmosphere was not critical. The run period at temperature was 60 days. The 85°C temperature was chosen to determine if corrosion due to moisture and other contaminants was a significant hazard in this temperature range. This test is intended to reveal the nature of the corrosion process and its dependence on bias. Tests were also done at 120°C. This temperature is above the range at which electrolytic corrosion is significant, yet 120°C is typical of that used for military qualification testing. The choice is admittedly somewhat arbitrary. Biased and unbiased packaged FETs were used in both these medium temperature stress tests. Package styles were discussed in Section 4.1.

We had also hoped to do a 170°C test on packaged FETs to compare results with those of the 200°C chip tests and to provide a one-to-one comparison between vendor packaged and chip devices. The 170°C temperature would have been low enough to avoid problems with package reliability. However, due to preliminary losses and to an increase in average device costs due to acquiring more recent FETs, we did not have enough devices for adequate stress tests at 170°C.

These medium temperature tests were performed in commercial Blue M ovens purged with nitrogen. Oscillation suppression networks were built into the bias circuits. DC and RF characteristics and S-parameters of the packaged FETs were monitored periodically during the tests.

The test plan is shown in Table 6-1. As was the case with the high temperature constant stress tests on chip devices, we made no differentiation between the ambient test temperatures for the biased and unbiased groups of low-noise FETs. Because the stress temperatures are in the range of the operating temperatures, we have anticipated a low failure rate, if the devices were properly fabricated.

TABLE 6-1

MEDIUM TEMPERATURE STRESS TESTS ON PACKAGED FETs

FET Type	Number of Devices Tested			
	85°C		120°C	
	Low Noise Bias	No Bias	Low Noise Bias	No Bias
A-51	3	1	2	0
D-22	1	1	1	1
H-1A1	2	2	2	3
H-21	4	1	4	1
N-21	1	2	1	2
N-31	3	2	2	2
N-32	1	2	1	2
R-51	0	1	1	1
Totals	15	12	14	12

6.2 FAILURE ANALYSIS

Failure criteria for the medium temperature constant stress tests are the same as those for the high temperature constant stress tests. The criteria were discussed in Section 2.7. Again, only the DC failure criteria were used.

Table 6-2 shows the failures that have occurred. "B" means biased, and "U" means unbiased. Most of the "failures" happened during test and handling procedures. There are too few device electrical failures to infer any failure statistics. The tests are continuing.

The failed packaged Type N-32 FET that was stressed biased at 120°C for 96 hours was delidded and examined. Extensive formation of the aluminum/gold intermetallic compound was discovered. The final report of the RADC/Hughes Failure Mechanism Study discusses this failure in detail and presents SEM photographs of the failed device.[1]

TABLE 6-2

MEDIUM TEMPERATURE CONSTANT STRESS TEST FAILURES

FET Type	Temp °C	FETs Started		FETs Failed		Principal Failure Mode						Hours to Failure	
						Test/ Handling		Gate Control		Gate Short			
		B	U	B	U	B	U	B	U	B	U	B	U
A-51	85	3	1	1	1	1	1					0	0
D-22	85	1	1	1						1		1764	
H-1A1	85	2	2	1		1						1764	
H-21	85	4	1		1				1				1764
N-21	85	1	2										
N-31	85	3	2		1						1		1764
N-32	85	1	2										
R-51	85		1										
A-51	120	2											
D-22	120	1	1	1	1		1			1		369	345
H-1A1	120	2	3										
H-21	120	4	1	1		1						345	
N-21	120	1	2	1						1		369	
N-31	120	2	2	1		1						345	
N-32	120	1	2	1						1		96	
R-51	120	1	1	1	1	1	1					345	345
Total		29	24	9	5	5	3		1	4	1		

7.0 RF CONSTANT STRESS TESTS ON PACKAGED FETs

7.1 RF STRESS TEST DESIGN

As a major goal of the reliability program is to be able to predict the mean time to failure of the low-noise FETs under actual operating conditions, it is vital that data on FETs stressed only by DC bias be supplemented by data on FETs that have also been subjected to RF drive power. As the RF stress tests are just now getting started, this section will mainly describe our plans. RF stress test data will become available later.

Each device to be tested is mounted in a microwave integrated circuit as an amplifier that is matched on input and output so as to achieve maximum output voltage and current swing. The tests are carried out at a baseplate temperature selected to facilitate comparison with the results of the high temperature constant stress tests on chips at DC bias. Consequently, no allowance was made for the DC bias power. Nor was any temperature rise due to RF power dissipation considered for these low-noise devices. The baseplate temperature must be sufficiently high to accelerate failure mechanism, yet be low enough so that the life test is on the FETs, not on the associated amplifier circuits and hardware. The test temperature that we have selected is 200°C.

Special RF test ovens have been built for the RF constant stress test. The basic design is similar to that of the DC bias ovens shown in Figure 5-1. Each oven is designed to hold up to ten amplifier housings that contain the FETs, plus input and output matching circuits. Bias networks and filters were incorporated in the drain and gate circuits. The source is grounded. Packaged devices were used, as construction of the amplifiers is facilitated for packaged FETs.

The RF system for these tests consists of a signal generator and 10W TWT power amplifier driving coaxial power splitters at 5.7 GHz. This frequency was chosen because it is near the highest for which low cost power splitters are available. At higher frequencies the cost is several times higher. The FETs have been selected and amplifier circuits have been designed to operate at this frequency. Adjustable pads on the inputs were used to set precisely the RF drive power.

Each amplifier was housed in its own covered case and was a self-contained unit with alumina microstrip tuning circuits and bias networks integral to the amplifier. The amplifier housing was mounted in the oven and was fed and terminated via high temperature coaxial line segments. The length of these segments was sufficient so that the temperature of critical input and output circuit components can be kept near room ambient.

This arrangement allows all DC and RF measurements to be made at the stress temperature. The amplifier in the oven is not disturbed. Concerns about handling damage, mechanical wear of the components, and possible variability of making the connections are therefore minimized.

Each output port was terminated by a coaxial attenuator, followed immediately by a Type N 50-ohm load. Measurements of RF power output were made by replacing the 50-ohm load with the sensing head of a precision RF power meter. Calibration of the system assures confidence in the measured results. By turning the coaxial attenuator from minimum to maximum attenuation while the load is being changed, we were able to measure the RF power output with the FET at the stress temperature without turning down the DC bias or RF power input. Thus, the principle of not disturbing a life test was closely followed.

7.2 SELECTION OF FETS FOR RF STRESS TEST

As shown in Table 2-1, seventeen packaged FETs have been set aside for the RF stress test. It should be noted that our reserves of these devices are very low. In addition, we have recently acquired three additional FETs of a type that we have designated Type E-1. This type device is a low noise packaged GaAs FET with a gate length of 0.5 μm and a gate width of 300 μm.

Although earlier we had planned to place twenty FETs on the RF stress test, for reasons explained below our present plans call for testing twelve devices, as shown in Table 7-1. Additional unexpected device losses may yet force a revision of the current plan.

TABLE 7-1

PLANNED 5.7 GHz RF CONSTANT STRESS TESTS
ON PACKAGED FETs

Oven No.	Type Code	Temp °C	No. FETs
RF-1	D-11	200	3
RF-2	H-1A1	200	3
RF-3	N-32	200	3
RF-4	E-1	200	3
TOTAL			12

The Type R-51 FETs will not be given the RF stress test, because of inherent problems with the lot of devices that we have procured. For example, Section 4.3 describes a Type R-51 FET that had source bond wires corroded from the eutectic die bonding material. Two of the four Type R-51 FETs originally scheduled for RF life test were mounted ready for RF life testing. However, a preliminary check of their RF characteristics indicated anomalous behavior. They were delidded, and both were found to have corroded source bond wires, similar in appearance to the source bond wires shown in Figure 4-5.

A third, pristine Type R-51 FET was delidded, and it also had corroded source bond wires. There seemed to be little point in subjecting Type R-51 FETs to further testing, and they were therefore deleted from the RF test plan.

We discovered another, more serious difficulty. When the RF stress test was being set up initially, an amplifier incorporating a Type N-32 FET was used in an oven to check out the system. After we were satisfied with the performance of the system at room temperature, we began heating the oven. We monitored the RF power output, and observed that the power started dropping off drastically as the temperature rose past about 150°C. Puzzling results were also obtained with a second Type N-32 FET. Symptoms indicated a loss of RF power input to the FET.

Consideration of the situation led to discovery that the miniature coaxial connectors on the amplifier housings were the source of the problem. On some connectors the solder was melting below 200°C. We sectioned a failed connector and could see clearly that the solder had flowed due to heating in our oven. When purchasing the connectors, we had specified high temperature connectors to be fabricated with SN10, an alloy of 87.9% lead, 10% tin, and 2.1% silver, with minimum melting point 268°C. However, an EDAX scan of the solder disclosed a different composition. We were able to use two sets of the connectors. The rest of the lot has been returned to the manufacturer for rework or replacement.

In the investigation of what turned out to be a connector problem, two type N-32 FETs were destroyed, along with one Type H-1A1 FET. Our inventory of devices for the RF stress test has thus decreased. Furthermore, we face a time delay in awaiting arrival of the replacement connectors. Consequently, we have decided to structure the RF stress test to use 12 FETs, consisting of three units each of four types from four different manufacturers, as shown in Table 7-1.

7.3 RF STRESS TEST RESULTS

We were able to place two FETs on the RF stress test. One Type E-1 device was mounted in the standard amplifier configuration on a microstrip line with matching input and output sections containing bias networks. To stabilize the device parameters, the FET was burned in at 200°C for two days.

At room temperature the amplifier was tuned to its operating frequency of 5.7 GHz. With -5 dBm power input, measurements showed a gain of 7.5 dB. Frequency purity was monitored with a spectrum analyzer. Bias was set at 3V drain voltage and 32 mA drain current with -0.55V on the gate. A power input level of +5.5 dBm resulted in 1 dB gain compression. With -5 dBm power input the 1 dB bandwidth was 230 MHz, offset 35 MHz toward the low side. The 3 dB bandwidth was 475 MHz.

As the temperature was increased to the stress level of 200°C, the gain decreased to about 5 dB. The bandwidth remained substantially unchanged. As of the writing of this report, several weeks of operation have been monitored with no changes having been observed in device operation.

The second FET to be placed on the RF stress test was a Type D-11 FET. Conditions of the test are similar to those for the Type E-1 FET. Over a period of a few weeks, the RF power output has changed by not more than 0.2 dB.

Additional FETs will be placed on the RF constant stress test, according to the schedule outlined in Table 7-1. As all devices will be burned in initially, based on the discussion of Section 5.8, we anticipate that the failure rates of the RF stress test devices will be fairly low at 200°C.

8.0 SUMMARY

We have investigated the reliability and operating life characteristics of commercially available, low noise, small signal, microwave, n-channel, gallium arsenide, metal-epitaxial-semiconductor field effect transistors with a Schottky-barrier gate. In total, 477 FETs representing both chip and packaged devices were procured for the study. Samples of representative chip types were optically photographed and given SEM/EDAX examinations.

DC, RF, and S-parameter measurements were made, including minimum noise figure and associated gain at 10 GHz. Failure criteria were defined in terms of changes in DC parameters.

A discussion was given of preliminary device losses. The results of environmental characterization studies were given. FETs were subjected to temperature cycling, acceleration, random vibration, mechanical shock, and hermeticity tests. We recommended that careful consideration be given to device selection, incoming inspection, and screening.

The major effort on the program was the high temperature constant stress tests on FET chips. In total, 137 FET chips were placed in specially designed ovens and subjected to a constant elevated temperature for a length of time. The temperatures used were 200°C, 220°C, 240°C, and 260°C. Eight FET types from six different manufacturers were used. DC bias was applied to 98 chips, while 39 chips remained unbiased.

A study was made of device degradation at the elevated temperature. A recommendation was made that an appropriate burn-in procedure be specified.

Device failures related to temperature were segregated for failure analysis and statistical studies. Log-normal plots were presented for selected runs, and mean time to failure was determined at the various test temperatures. An Arrhenius plot was given for biased Type N-3 devices. A discussion of the effects of various test designs was given. The Type N-3 FET was estimated to have a mean time to failure at normal operating temperatures in the range of 10^7 to 10^8 hours. We recommended that failure limits be carefully defined with the specific application in mind.

The results of RF and S-parameter measurements on FETs from the high temperature tests were discussed briefly.

Fifty-three packaged FETs were subjected to medium temperature constant stress tests. Eight device types from five different manufacturers were represented. Two temperatures were used, 85°C and 120°C. Twenty-nine of the devices were placed under low-noise bias. To date, insufficient numbers of device failures have occurred to enable us to reach any conclusions about reliability characteristics. The tests are continuing.

RF constant stress tests on packaged devices are just now getting started. The test plan calls for stressing 12 FETs, representing four device types from four different manufacturers. The baseplate temperature will be 200°C. The devices will be operated as matched amplifiers at a frequency of 5.7 GHz. Two FETs have been operated in an RF test oven for several weeks now, with no significant change in parameters. Additional devices will be RF tested.

In conclusion, five observations are in order. First, the program was construed as being an extensive study rather than an intensive one. Thus, we tested many devices in many different ways. However, few in-depth studies of specific device types were made, due to lack of sufficient numbers of devices of any one type. We have therefore been able to raise a number of issues that await resolution in an intensive study program.

Second, we felt that the overall purpose of the program was best served by taking devices as received and committing them to the tests. This procedure gives good raw failure data. However, it does not correspond to industry practice. Different reliability results would be expected for devices tested appropriately for a specific systems application.

Third, we have completed the work on the program using what we initially thought were expeditious ways for obtaining and handling the test data. In future programs, however, we would strongly recommend automated testing methods wherever possible. These should be interfaced with a digital data storage, manipulation, and retrieval system. Such a system would greatly aid in updating status files and would also be useful in program planning and management.

Fourth, and most important, the timely assignment of appropriate, qualified people to the program was vital to the formation of a capable team to accomplish the program goals. We have felt continued support and encouragement from Hughes' management and from the cognizant people at the Rome Air Development Center.

Finally, although numerous failures have been documented in the program, no vendor's product should be rejected because of these studies. Of necessity to accelerate the failure processes, the devices were subjected to stresses typically far in excess of the manufacturer's recommendations. As these tests were made on devices procured through normal commerical channels, there is no justification for the assumption that the reliability of the devices we tested is representative of the reliability of the manufacturer's best product.

Also, we tested devices that were for the most part fabricated two to three years ago. Every serious manufacturer that we know has taken steps to improve his product during that length of time. Therefore, even normal commercial transistors purchased from the current catalog will likely show improvements over the devices that we tested. We are pleased to state in every case where we contacted a vendor regarding what we thought might have been a processing problem with a particular shipment of FETs, that the vendor sent us replacement devices without delay.

We have concluded that systems designers can now reliably specify the use of appropriately qualified low noise gallium arsenide field effect transistors.

9.0 REFERENCES

1. L. S. Bowman and W. Tarn, "Failure Mechanism Study of GaAs FET Technology", Hughes Aircraft Company Torrance Research Center, Torrance, CA 90509, Final Report, Contract No. F30602-78-C-0326, Rome Air Development Center, Griffiss AFB, NY 13441.

2. R. Lundgren, "Reliability Study of GaAs FET", Hughes Research Laboratories, Malibu, CA 90265, Final Report, June 1978, Contract No. F30602-76-C-0374, Rome Air Development Center, Griffiss AFB, NY 13441.

3. T. Irie, I. Nagasako, H. Kahzu, and K. Sekido, "Reliability Study of GaAs FETs," IEEE Transactions, MTT-24, No. 6, pp. 321-328 (June 1976).

4. D. S. Peck and O. D. Trapp, Accelerated Testing Handbook, published by Technology Associates, 51 Hillbrook Drive, Portola Valley, CA 94025, and The Bell Telephone Laboratories, Murray Hill, NJ 07974.

APPENDIX A

TABLE SHOWING STATUS OF CHIP DEVICES FOR HIGH TEMPERATURE CONSTANT STRESS TESTS

Table A-1 gives detailed information on every FET chip that was given a serial number prior to assignment to a high temperature oven. The "Run No." identifies a specific oven loading listed in Table 5-1.

TABLE A-1

STATUS OF CHIP DEVICES FOR HIGH TEMPERATURE CONSTANT STRESS TESTS

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
1	N-3	2	200				0		DC short
2	N-3	2	200	1	B		881.1		Damaged during handling
3	N-3	2	200				0		No V_P
4	N-3	2	200	1	B		881.1	ΔI_{DS}	
5	N-3	2	200	1	B		881.1	ΔI_{DS}	
6	N-3	2	200	1	B		599	High gate current I_G	
7	N-3	2	200	1	B		2811.6		Carrier broken
8	N-3	2	200	1	B		881.1	High gate current I_G	
9	N-3	2	200	1	B		881.1	ΔI_{DS}	
10	N-3	2	200	1	B		881.1	ΔI_{DS}	
11	N-3	2	200	1	B		881.1	ΔI_{DS}	
12	N-3	2	200	1	B		2811.6	S/D short	

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
13	N-3	2	200	1	U		1464.9	ΔI_{DS}	
14	N-3	2	200	1	U		1464.9	ΔI_{DS}	
15	N-3	2	200	1	U	2811.6			
16	H-1	1	200	2	U		361	ΔI_{DS}	
17	H-1	1	200	2	B		1645		G/S short during DC test
18	H-1	1	200	2	B		906.7	High gate current I_G	
19	H-1	1	200	2	B	3159.3			
20	H-1	1	200	2	B		361		FET chip delaminated
21	H-1	1	200	2	B		361	ΔI_{DS}	
22	H-1	1	200				0		Failed at initial RF test
23	H-1	1	200	2	B		1645		Carrier cracked
24	H-1	1	200	2	U		361	ΔI_{DS}	

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
25	H-1	1	200	2	B		906.7	ΔI_{DS}	
26	H-1	1	200	2	U		361	ΔI_{DS}	
27	H-1	1	200	2	B		3159.3	S/D short	
28	H-1	1	200	2	U	3159.3			
29	H-1	1	200	2	B		1645	No V_P	
30	H-1	1	200	2	U		361	ΔI_{DS}	
31	H-1	1	200	2	B		361	ΔI_{DS}	
32	H-1	3	220	3	U		1282.4	S/D short	
33	H-1	3	220	3	B		262.8	ΔI_{DSS}	
34	H-1	3	220	3	U		1282.4	ΔI_{DS}	
35	H-1	3	220	3	U		846.4	ΔI_{DS}	
36	H-1	3	220	3	B		262.8	ΔI_{DS}	
37	H-1	3	220	3	B		262.8	ΔI_{DS}	
38	H-1	3	220	3	B		486.1		Carrier cracked

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
39	H-1	3	220	3	B		262.8	ΔI_{DS}	
40	H-1	3	220	3	B		262.8	ΔI_{DS}	
41	H-1	3	220	3	B		262.8	ΔI_{DS}	
42	H-1	3	220	3	U		262.8	ΔI_{DS}	
43	H-1	3	220	3	B		262.8	ΔI_{DS}	
44	H-1	3	220	3	B		262.8	ΔI_{DS}	
45	H-1	3	220	3	B		262.8	ΔI_{DS}	
46	N-3	2	200	1	U		881.1	ΔI_{DS}	
47	N-3	4	220	4	B		426.1	S/D short	
48	N-3	4	220	4	B		426.1		Switching transient blew device at I_{DSS} test
49	N-3	4	220	4	B		1300.9	ΔI_{DS}	
50	N-3	4	220	4	U		426.1	ΔI_{DS}	

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
51	N-3	4	220	4	B		426.1	ΔI_{DS}	
52	N-3	4	220	4	B		426.1	ΔI_{DS}	
53	N-3	4	220	4	B		426.1		G/S short appeared at RF test
54	N-3	4	220	4	B		426.1	ΔI_{DS}	
55	N-3	4	220	4	U		426.1	ΔI_{DS}	
56	N-3	4	220	4	B		64.9	ΔI_{DS}	
57	N-3	4	220	4	B		426.1	ΔI_{DS}	
58	N-3	4	220	4	B		426.1		Carrier broken
59	N-3	4	220	4	U		426.1	ΔI_{DS}	
60	N-3	4	220	4	U		426.1	ΔI_{DS}	
61	N-3	4	220	4	B	1300.9			
62	P-5	6	240				0		Chip void - couldn't mount

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
63	P-5	6	240				0		Chip void - couldn't mount
64	P-5	6	240				0		Initial test No V_P
65	P-5	6	240				0		Initial test No V_P
66	P-5	6	240	5	B		318	High gate current	
67	P-5	6	240	5	B		318	High gate current	
68	P-5	6	240	5	B		318	High gate current	
69	P-5	6	240	5	B		318	High gate current	
70	P-5	6	240	5	U		24	S/D short	
71-79	R-5								Had trouble bonding. Wouldn't test

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
80-88	N-2						0		Bond pad lifted
89	D-2	5	240	6	B		1094.9	ΔI_{DS}	
90	D-2	5	240	6	B	1094.9			
91	D-2	5	240	6	B		1094.9	ΔI_{DS}	
92	D-2	5	240				0		Carrier cracked
93	D-2	5	240				0		Bond pad lifted
94	D-2	5	240				0		Bond pad lifted
95	D-2	5	240	6	B		1094.9	ΔI_{DS}, I_{DSS}	
96	D-2	5	240	6	B		1094.9	ΔI_{DS}, I_{DSS}	
97	D-1	5	240	6	U		1094.9	ΔI_{DS}	
98	D-1	5	240	6	B		1094.9	ΔI_{DS}	
99	D-1	5	240	6	B		1094.9	ΔI_{DS}	
100	D-1	5	240	6	B		1094.9	S/D short	

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
101	D-1	5	240	6	B		1094.9	ΔI_{DS}, I_{DSS}	
102	D-1	5	240	6	U		1094.9	ΔI_{DS}, I_{DSS}	
103	D-1	5	240	6	B		257.4		Carrier broken
104	A-6	7	220				0		Very unstable I_G
105	A-6	7	220				0		Initially no family
106	A-6	7	220	7	B		1223.1	ΔI_{DS}	
107	A-6	7	220	1	B		1223.1	ΔI_{DS}	
108	A-6	7	220	7	B		1223.1	ΔI_{DS}	
109	A-6	7	220	7	B		1223.1	ΔI_{DS}	
110	A-6	7	220				0		Device damaged in handling
111	A-6	7	220	7	B		1223.1		Wire bonds damaged in handling
112	A-6	7	220	7	B		1223.1	ΔI_{DS}	

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
113	A-6	7	220	7	B		1223.1	ΔI_{DS}	
114	A-6	7	220	7	B		1223.1	ΔI_{DS}	
115	A-6	7	220	7	U		1223.1	ΔI_{DS}	
116	A-6	7	220	7	B		1223.1	ΔI_{DS}	
117	A-6	7	220	7	B		1223.1	ΔI_{DS}	
118	A-6	7	220	7	U		1223.1	ΔI_{DS}	
119	A-6	6	240	8	B		1275.6	ΔI_{DS}	
120	A-6	6	240	8	B		1275.6	ΔI_{DS}	
121	A-6	6	240	8	B		1275.6	ΔI_{DS}	
122	A-6	6	240	8	B		1275.6	ΔI_{DS}	
123	A-6	6	240	8	B		100.3		Carrier broken
124	A-6	6	240	8	B		1275.6	ΔI_{DS}	
125	A-6	6	240				0		V_{GS} short - Never in oven
126	A-6	6	240	8	B		1275.6	ΔI_{DS}	

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
127	A-6	6	240	8	B		1275.6	ΔI_{DS}	
128	A-6	6	240	8	B		1275.6	ΔI_{DS}	Carrier broken
129	A-6	6	240	8	B		1275.6	ΔI_{DS}	
130	A-6	6	240	8	U		1275.6	ΔI_{DS}	
131	A-6	6	240	8	U		1275.6	ΔI_{DS}	
132	A-6	6	240				0		No V_P - Never in oven
133	A-6	6	240	8	U		1275.6	ΔI_{DS}	
134	A-6	1	260				0		Initial short at RF
135	A-6	1	260	9	B		533.3	ΔI_{DS}	
136	A-6	1	260	9	U		533.3	ΔI_{DS}	
137	A-6	1	260	9	B		533.3	ΔI_{DS}	
138	A-6	1	260	9	B		533.3	ΔI_{DS}	
139	A-6	1	260				0		Initial test No V_P

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
140	A-6	1	260	9	B		533.3	ΔI_{DS}	
141	A-6	2	260	9	U		533.3	ΔI_{DS}	
142	A-6	2	260	9	U		533.3	ΔI_{DS}	
143	A-6	1	260	9	U		533.3	ΔI_{DS}	
144	N-3	7	260	12	B		48	ΔI_{DS}	
145	N-3	7	260	12	B		159.6		Handling Accident
146	N-3	7	260	12	U		48	ΔI_{DS}	
147	N-3	7	260	12	B		48	ΔI_{DS}	
148	N-3	7	260	12	B		48	ΔI_{DS}	
149	N-3	7	260	12	U		48	ΔI_{DS}	
150	N-3	7	260	12	B		48	ΔI_{DS}	
151	N-3	7	260		-		0		High I_G - Never in oven
152	N-3	7	260	12	U		48		Handling Accident

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
153	N-3	7	260	12	B		48	ΔI_{DS}	
154	N-3	7	260	12	B		48	ΔI_{DS}	
155	N-3	7	260		-		0		Initial No V_P
156	N-3	7	260		-		0		Initial No V_P
157	N-3	7	260	12	U		48	Δg_m	
158	A-10	1	260		-		0		Physically Lost
159	A-10	1	260	10	B		163.2		Bond Pad Lifted
160	A-10	1	260		-		0		Carrier Broken
161	A-10	1	260	10	B		163.2		Carrier Broken
162	A-10	1	260	10	U		307.2		Handling Accident
163	A-10	1	260		-		0		Bond Pad Lifted
164	A-10	1	260	10	B	307.2			

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
165	A-10	1	260	10	B		307.2		Handling Accident
166	A-10	1	260		-		0		Initial No V_P
167	A-10	1	260	10	B		163.2	S/D short	
168	A-10	1	260	10	U	307.2			
169	A-10	1	260		-		0		Bond Pad Lifted
170	A-10	1	260		-		0		Bond Pad Lifted
171	A-10	1	260	10	U		163.2	ΔI_{DS}	
172	H-11	6	260	11	B		96	ΔI_{DSS}	
173	H-11	6	260	11	B		96	No V_P	
174	H-11	6	260	11	B		144	ΔI_{DSS}	
175	H-11	6	260	11	U		96	G/S short	
176	H-11	6	260	11	B		48		Missing @ 2 Days
177	H-11	6	260	11	B		96		Mechanical Damage

TABLE A-1 (CONTINUED)

Serial Number	Type Code	Oven No.	Temp °C	Run No.	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Induced Failures	Other Failures
178	H-11	6	260	11	U		96	ΔI_{DSS}	
179	H-11	6	260		-		0		Carrier Broken
180	H-11	6	260		-		0		Initial RF Short
181	H-11	6	260	11	B		144	Δg_m	
182	H-11	6	260	11	U		48	ΔI_{DSS}	
183	H-11	6	260	11	B		48	High V_{GS} - In Oven	
184	H-11	6	260	11	B		96	ΔI_{DS}	
185	H-11	6	260	11	B		144	No V_P	
186	H-11	6	260	11	U		48	ΔI_{DS}	

APPENDIX B

RECENT RESULTS OF RELIABILITY TESTING OBTAINED AFTER PREPARATION OF THE FINAL REPORT DRAFT

An addendum to the term of the contract was arranged to log additional time on the medium temperature and RF constant stress tests. The additional reliability information was obtained through November 1980 and is presented below as a supplement to the body of the report.

B.1 MEDIUM TEMPERATURE CONSTANT STRESS TESTS

B.1.1 Oven A at 85°C

With the subsequent addition of one biased Type A-51 FET at 85°C to the numbers of the devices shown in Table 6-1, sixteen low-noise biased FETs and twelve unbiased FETs were stressed at 85°C. All were packaged. At the end of the program some devices had remained within the limits of the failure criteria outlined in Section 2.7. The numbers of hours at 85°C logged by these FETs are shown in Table B-1 in the "Not Failed" column.

Other devices had failed, either by catastrophic occurrence or by change in a DC electrical parameter in excess of the specified limits. These failed FETs are identified, and the "Hours to Failure" are shown in Table B-1. Whether the failure seems to be primarily the result of the temperature stressing or not is also indicated. "Set up failure" means that the device was damaged physically or electrically during placement in the oven or subsequent application of bias. Devices with degradation failures continued to be temperature stressed beyond their non-catastrophic failure point in an attempt to accentuate the failure mechanism for easier identification.

It should be noted that device #8-B was carried in inventory as a Type D-22 FET. Delidding the package and examining the chip disclosed that the device was in fact a Type D-11 FET.

TABLE B-1

FINAL STATUS OF PACKAGED DEVICES FOR 85°C CONSTANT STRESS TEST

Serial Number	Type Code	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Related Failure	Other Failures
3	R-51	U		3,931	Open source	
6	H-21	B		1,457	I_{DSS}	
7	H-21	B		331	I_{DSS}	
8-A	H-21	B		331	I_{DSS}	
8-B†	D-11	B		1,764	G/S Short	
9-A	H-21	B		331	I_{DS}	
9-B	D-22	U		1,457	I_{DSS}	
10	H-21	U		1,764	Gate control	
12	A-51	B		3,931	Gate control	
13	A-51	B		3,148	I_{DS}	
16	A-51	B		0		Set up
17	N-21	U		1,457	I_{DSS}	
19	N-21	U		1,457	I_{DSS}	
20	N-21	B	4,221			
21-A	A-51	U		0		Set up
21-B	H-1A1	B		1,457	I_{DS}	
22	H-1A1	B		1,764		Lost
23-A	H-1A1	U		1,457	I_{DS}	
23-B	N-32	U	4,221			
26	N-32	U		1,457	I_{DSS}	
30	H-1A1	U		1,457	I_{DS}	
34-A	N-32	B	4,221			
34-B	A-51	B		1,457		Set up
41	N-31	B		1,457	I_{DS}	
42	N-31	B	4,221			
44	N-31	B	4,221			
73	N-31	U		1,764	G/S Short	
93	N-31	U		3,931	I_{DSS}	

†Note: See text.

A summary of the observed causes of failure for each device type is given in Table B-2. As was the case with FETs in the high temperature test, the primary failure category was excessive change in the drain current. Although insufficient failure information on any one device type is available for meaningful statistical analysis, the general discussions of Sections 5.4 and 5.8 on device degradation and the effects of test design seem to apply to the packaged FETs as well.

One valid conclusion about the packaged low-noise FETs can be reached. That is that devices manufactured by the N Company performed exceptionally well. This finding results from the facts that five of the eleven N-type devices survived the stress test and that no other manufacturer's devices survived. This conclusion does not mean that we find other manufacturer's devices inferior. Insufficient numbers of packaged devices were tested to reach definite statistical predictions of their reliability. Section 8.0 discusses the basis of the numbers and types of devices that were selected for the various tests on this program.

Failure analysis of FETs from the 85°C constant stress test is given in the companion Failure Mechanism Study.[1]

B.1.2 Oven B at 120°C

The numbers of the devices shown in Table 6-1 for the 120°C tests total fourteen low-noise biased FETs and twelve unbiased FETs. All were packaged. Similar to Tables B-1 and B-2, Tables B-3 and B-4 show for the 120°C oven the status of the FETs as of the end of the program and the categories of failures.

It should be noted that device #39 was carried in inventory as a Type N-32 FET. Delidding the package and examining the chip disclosed that the device was in fact a Type N-21 FET.

Compared to the 85°C results, the 120°C results showed fewer device failures at 1,457 hours. The primary failure mode was again the drain current exceeding the specification limits. Next in numbers of temperature-related failures was the catastrophic occurrence of gate-to-source short circuits.

TABLE B-2

CATEGORIES OF FAILURES IN 85°C CONSTANT STRESS TESTS ON PACKAGED DEVICES

Type Code	No. FETs Started		Not Failed		Set-Up Failures		Related to Temperature									
							Temperature Failures		Gate Control		Gate Short		Open Source		Drain Current	
	B	U	B	U	B	U	B	U	B	U	B	U	B	U	B	U
A-51	4	1			2	1	2		1						1	
D-11	1						1				1					
D-22		1						1								1
H-1A1	2	2			1		1	2							1	2
H-21	4	1					4	1		1					4	
N-21	1	2	1					2								2
N-31	3	2	2				1	2				1			1	1
N-32	1	2	1	1				1								1
R-51		1						1						1		
Totals	16	12	4	1	3	1	9	10	1	1	1	1		1	7	7

TABLE B-3

FINAL STATUS OF PACKAGED DEVICES FOR 120°C CONSTANT STRESS TEST

Serial Number	Type Code	Biased/ Unbiased	Not Failed, Hours	Hours to Failure	Temperature-Related Failure	Other Failures
1-A	H-21	B	2,439			
1-B	A-51	B		345	I_{DS}	
2-A	H-21	B	2,439			
2-B	R-51	U		345		Set up
3	H-21	B	2,439			
4-A	H-21	B		345		Set up
4-B	D-22	B		369	G/S Short	
4-C	R-51	B		345		Set up
4-D	A-51	B		345	I_{DS}	
5-A	H-21	U	2,439			
5-B	D-22	U		345		Set up
21	N-21	U		345	I_{DS}	
22	N-21	U		345	I_{DS}	
23	N-21	B		369	G/S Short	
28	N-31	U		2,439		Lost
33	H-1A1	B	2,439			
34	H-1A1	B		2,439	I_{DSS}	
36	H-1A1	U		345	I_{DS}	
37	H-1A1	U	2,439			
38-A	H-1A1	U		345	I_{DS}	
38-B	N-32	B		96	G/S Short	
39†	N-21	U		345	I_{DS}	
48	N-32	U	2,439			
75	N-31	B		345		Broken Lead
78	N-31	B	2,439			
79	N-31	U	2,439			

†Note: See text.

TABLE B-4

CATEGORIES OF FAILURES IN 120°C CONSTANT STRESS TESTS ON PACKAGED DEVICES

Type Code	No. FETs Started		Not Failed		Set-Up Failures		Related to Temperature									
							Temperature Failures		Gate Control		Gate Short		Open Source		Drain Current	
	B	U	B	U	B	U	B	U	B	U	B	U	B	U	B	U
A-51	2	0					2								2	
D-22	1	1				1	1				1					
H-1A1	2	3	1	1			1	2							1	2
H-21	4	1	3	1	1											
N-21	1	3					1	3			1					3
N-31	2	2	1	1	1	1										
N-32	1	1		1			1				1					
R-51	1	1			1	1										
Totals	14	12	5	4	3	3	6	5			3				3	5

A look at the "Not Failed" column in Table B-4 indicates that good performance was obtained from FETs supplied by the H Company and the N Company. As explained in Section B.1.1, we allow that other manufacturers also have good products. Comparison of the "Not Failed" columns in Tables B-2 and B-4 shows that N-type FETs should certainly be included with device types considered for critical systems applications.

Failure analysis of FETs from the 120°C constant stress test is given in the companion Failure Mechanism Study.[1]

B.2 RF CONSTANT STRESS TEST

B.2.1 Test Equipment

A description of the RF constant stress test was given in Section 7.1. Figure B-1 shows a photograph of the actual RF test installation. Two ovens are shown, each one configured for RF testing of five FET amplifiers. The DC terminal strips and sampling box are visible on the footplates. The tall device on the front right corner of each footplate is the nitrogen flow meter. A constant nitrogen purge was used to flush the oven and keep the amplifiers clean. The nitrogen derived from a liquid source, which was backed up with a tank that continued the flow in case the primary nitrogen supply was interrupted. When interruption occurred, an alarm sounded to alert the plant guard post. The guard then called one of us, and we shut down the test temporarily, if a long outage was anticipated. A timer told us how long nitrogen had been supplied from the tank.

Primary 60-Hz power to the RF life test equipment was supplied through a dedicated power and control panel, of which the nitrogen monitoring system was part. When the plant power failed, a sensitive circuit breaker operated within a few cycles to lock out the RF life test equipment, and the alarm sounded. Thereafter, restoration of 60-Hz power had to be accomplished manually. DC bias was, however, maintained on the FET gates by a battery in the gate bias supply box, shown on the shelf in the top center of Figure B-1. These procedures gave adequate safeguards to protect the FETs in case of unplanned power or nitrogen outages.

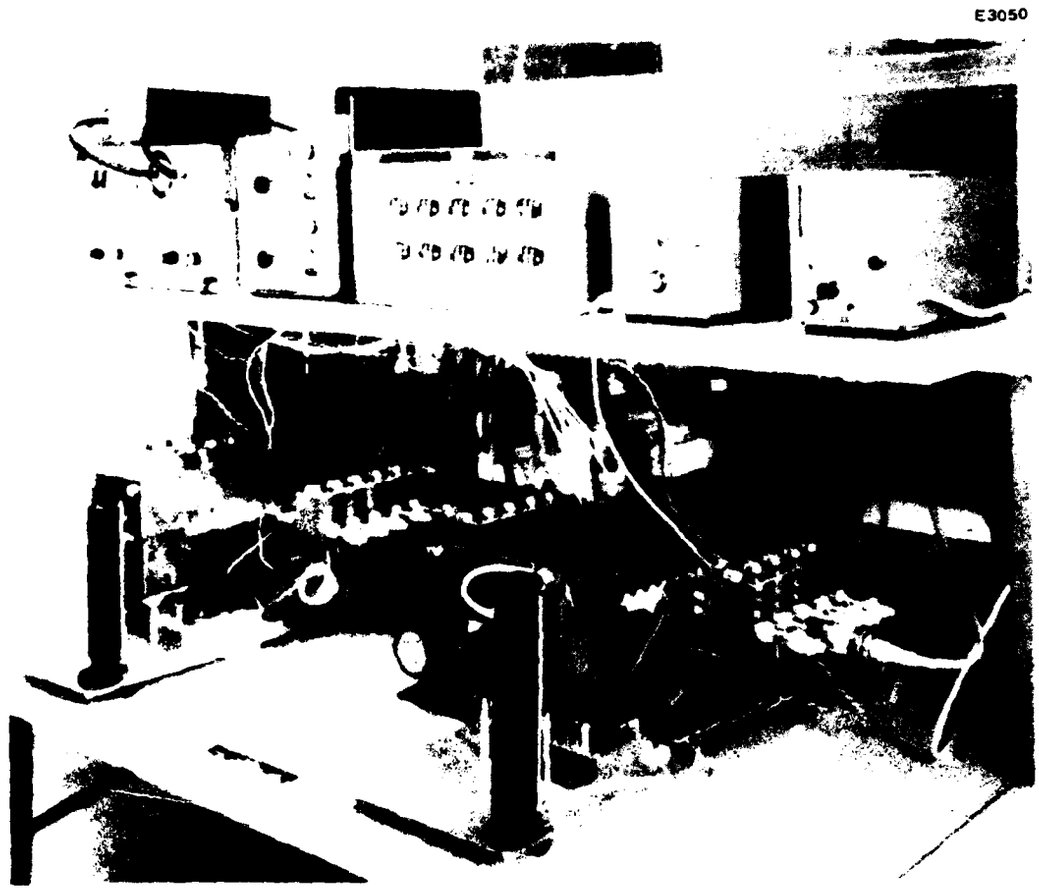


Figure B-1 RF constant stress test installation.

Also shown in Figure B-1 the shelf to the immediate left of the gate bias supply box are the data log book and the two oven temperature controllers. By the wall can be seen two Lambda power supplies furnishing drain bias for the two installations. A 1 kΩ, 2W carbon composition resistor is across the output terminals of each supply for stabilization. Above the Lambda power supplies are the Hughes Model 1177H Traveling Wave Tube (TWT) amplifier and the General Microwave signal generator set at 5.69 GHz. For light loading, adequate convection cooling of equipment was afforded in the stacked configuration.

Two Hewlett-Packard RF power meters are located on the shelf to the right of the gate bias supply box. Ten gate bias leads are shown attached to the box. The gate and drain bias leads are spatially spread to reduce coupling between them and to prevent bias circuit oscillations.

RF output from the TWT amplifier was carried behind the shelf by coaxial cable to Microlab/FXR power splitters mounted underneath the shelf. Individual attenuators in each circuit were adjusted to provide the proper RF input power level to each amplifier in the ovens. An RF input power level of -5 dBm was used for the Type E-1 FET; -10 dBm was used for all other devices. RF input power drift did not exceed 0.1 dB. In Figure B-1 five FET amplifiers are operating in the left oven and two in the right oven, with three positions unused. On the output side of the ovens additional attenuators and 50-ohm terminations complete the RF circuit. Figure B-1 shows the RF power head monitoring RF output power on one channel.

B.2.2 Early RF Stress Test Results

As explained in Section 7.2, we have deleted the packaged Type R-51 FETs from the RF constant stress test, because on several devices we have encountered corrosion of the source bond wires due to wetting by the eutectic die bond solder. Figure 4-5 depicts the problem on the same device type from the environmental test sequence. SEM photographs of two delidded Type R-51 FETs originally scheduled for the RF constant stress test show similar source bond wire deterioration. The SEM photographs and additional details concerning these failed FETs are given in Appendix A of the Failure Mechanism Study.[1]

The solder flow problem in the miniature coaxial connectors that was mentioned in Section 7.2 has been corrected by the manufacturer. Tests showed that the reworked connectors would withstand at least 250°C, and they were installed on all RF oven housings. However, the work described in the next paragraph was done with the old, but good, connectors.

Considerable time under DC bias with RF input at the 200°C stress temperature was logged on both the Type E-1 and Type D-11 FETs. The specific conditions of the test were described in Section 7.3. The Type E-1 FET accumulated 1438 hours of operation, and the Type D-11 logged 1087 hours. Regular measurements, usually three times per week, were made of the RF input power and output power. During operation at 200°C the RF output power from the Type E-1 FET had changed by less than 0.1dB. The RF output power from the Type D-11 FET had changed not more than 0.5 dB. These tests were terminated when it became necessary to cool the oven in preparation for mounting additional RF test housings on the heater block.

The Type E-1 FET did not fail during the RF constant stress test. Subsequent testing disclosed a leaky gate diode characteristic. The package was delidded and the FET was examined under the SEM. The aluminum gate had a ragged appearance. Voids in the surface gold of the drain and source metallizations were also noted. Details of the observations accompanied by SEM photographs are given in Appendix A of the final report for the Failure Mechanism Study. [1]

Three additional packaged FETs of Type E-1 from a different lot were DC tested prior to being placed on the RF life test at 200°C. All three had a leaky gate diode characteristic and were withdrawn from testing and delidded. The gate and drain metallizations had appearances similar to those of the stressed FET. In a separate experiment we determined that overheating of the device during assembly caused voids in the gold metallization.

Based on our results with four devices, it was apparent that the fabrication procedures for the Type E-1 FETs were still in the process of improvement. Consequently, as the manufacturing process had not been fixed, life testing the current lots of devices would have resulted in no usable reliability data. The Type E-1 FETs were therefore deleted from the RF stress testing program.

The Type D-11 FET also did not fail during the RF constant stress test. However, having logged over 1000 hours at 200°C at the time the oven was cooled, the device was removed from the oven and examined. DC testing showed a leaky gate diode characteristic and excessive pinch-off voltage. The package was then delidded. A slight pitting of the gold metallization was observed. No other indication of possible degradation was present. Based on our experience with life testing the Type E-1 and Type D-11 devices, we proceeded with testing the remaining FETs.

One Type N-32 FET was destroyed in mounting. The remaining FETs listed in Table 7-1 underwent the RF constant stress test at 200°C baseplate temperature.

B.2.3 Final RF Stress Test Results

Besides testing one Type E-1 FET and one Type D-11 FET, as was reported in the previous section, we were able to test seven additional devices, as shown in Figure B-1. In the left oven are three Type H-1A1 FETs and two Type D-11 FETs. The right oven contains two Type N-32 devices. Table B-5 lists the final status of the nine packaged devices that were stress tested with RF input and 200°C baseplate temperature. The RF input level was below the gain saturation point of the FETs. Failure criteria were taken from Table 2-8. All failures were of the gradual degradation type, and no effects that could be ascribed specifically to the RF input were observed.

As shown in Table B-5, the degradation modes of the last seven devices were device specific. The two Type D-11 FETs failed by having the specific drain current I_{DS} and saturated drain current I_{DSS} change excessively. The RF gain remained within specification.

One Type H-1A1 FET had excessive changes in I_{DS} and I_{DSS}, while these parameters remained within specification for the other two Type H-1A1 devices. The RF gain remained within specification on all three Type H-1A1 FETs.

The measured DC parameters remained within specification for the Type N-32 FETs. RF gain remained unchanged.

TABLE B-5

STATUS OF PACKAGED DEVICES WHEN THE

200°C RF STRESS TEST WAS TERMINATED

Serial Number	Type Code	Not Failed, Hours	Hours to Failure	RF Gain, dB		Failure Mode
				Initial	Final	
1R	E-1		1438	5.4	5.4	Leaky gate
2R	D-11		1087	6.8	6.4	Leaky gate
3R	H-1A1		477	3.6	2.9	ΔI_{DS}, ΔI_{DSS}
4R	H-1A1	477		1.8	1.2	
5R	H-1A1	477		2.0	1.3	
6R	D-11		477	4.0	3.5	ΔI_{DS}, ΔI_{DSS}
7R	D-11		477	4.6	4.6	ΔI_{DS}, ΔI_{DSS}
8R	N-32	452		4.0	4.0	
9R	N-32	452		4.0	4.0	

The reliability investigation of FETs under temperature stress with normal RF power applied gave results similar to the medium power FET reliability tests reported in Section B-1. Best performance was obtained from the Type N-32 FETs, with the Type H-1A1 devices a close second. Including the Type D-11 FETs, no device exceeded the RF failure criterion of - 1 dB change in gain.

Failure mechanism studies of the #1R and #2R devices are given in the companion Failure Mechanism report[1]. Device types included in FETs #3R through #9R already have been comprehensively analyzed in the high and medium temperature stress investigations. We did not expect that any new, useful reliability information would emerge from demantling these devices and subjecting them to more study, as none of the devices had failed catastrophically or even had more than nominal degradation in drain current. Therefore, these devices were not delidded and examined further, but were retained intact for subsequent use.

MISSION
of
Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.

END

DATE
FILMED
1-82

DTIC